W65C365

PRELIMINARY

INFORMATION, SPECIFICATION AND DATA SHEET

W65C365
84 LEAD
CHIP CARRIER

Top side

Pin	Signal
11	P67/TXD3
10	P66/RXD3/NE66
9	P65/TXD2
8	P64/RXD2/NE64
7	P63/TXD1
6	P62/RXD1/PWM
5	P61/TXD0/TOUT
4	P60/RXD0/TIN
3	P57/PID7/NE57
2	P56/PID6/PE56
1	VSS
84	VDD
83	P55/PID5
82	P54/PID4
81	P53/PID3
80	P52/PID2
79	P51/PID1
78	P50/PID0
77	P47/PIRS2
76	P46/PIRS1
75	P45/PIRS0

Left side

Pin	Signal
12	RES-
13	WE-
14	RUN/SYNC
15	FCLKO-
16	FCLK
17	BE/RDY
18	CLK
19	CLKO-
20	PHI2
21	BA/DOD-
22	VSS
23	VDD
24	P00/A0
25	P01/A1
26	P02/A2
27	P03/A3
28	P04/A4
29	P05/A5
30	P06/A6
31	P07/A7
32	P10/A8

Right side

Pin	Signal
74	P44/PICS-/PIRD-
73	P43/PIWE-/PIWR-
72	P42/PII-
71	P41/IRQ-
70	P40/NMI-/ABORT-
69	TG1
68	TG0
67	P27/D7
66	P26/D6
65	P25/D5
64	VSS
63	VDD
62	P24/D4
61	P23/D3
60	P22/D2
59	P21/D1
58	P20/D0
57	P77/CS7-
56	P76/CS6-
55	P75/CS5-
54	P74/CS4-

Bottom side

Pin	Signal
33	P11/A9
34	P12/A10
35	P13/A11
36	P14/A12
37	P15/A13
38	P16/A14
39	P17/A15
40	P30/A16
41	P31/A17
42	P32/A18
43	VSS
44	VDD
45	P33/A19
46	P34/A20
47	P35/A21
48	P36/A22
49	P37/A23
50	P70/CS0-
51	P71/CS1-
52	P72/CS2-
53	P73/CS3-

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TABLE OF CONTENTS

TABLE OF CONTENTS

FIGURES

TABLE OF CONTENTS

TABLES

INTRODUCTION

The WDC W65C365 microcomputer is a complete fully static 32-bit computer fabricated on a single chip using a Hi-Rel low power CMOS process. The W65C365 complements an established and growing line of W65C products and has a wide range of microcomputer applications. The W65C365 has been developed for Hi-Rel applications and where minimum power is required.

The W65C365 consists of a W65C832S (Static) Central Processing Unit (CPU), 8K bytes of Read Only Memory (ROM), 576 bytes of Random Access Memory (RAM), Processor defined cache under software control, eight 16-bit timers with maskable interrupts, high performance interrupt driven Parallel Interface Bus (PIB), four Universal Asynchronous Receivers and Transmitters (UART) with baud rate timers, Monitor "Watch Dog" Timer with "restart" interrupt, twenty-nine priority encoded interrupts, ICE Interface, Time of Day (ToD) clock features, Twin Tone Generators (TGx), Bus Control Register (BCR) for external memory bus control, interface circuitry for peripheral devices, and many low power features.

The innovative architecture and the demonstrated high performance of the W65C832S CPU, as well as instruction simplicity, result in system cost-effectiveness and a wide range of computational power. These features make the W65C365 a leading candidate for 32-bit microcomputer applications especially where task oriented processing is desired.

This product description assumes that the reader is familiar with the W65C832 CPU hardware and programming capabilities. Refer to the W65C832 Data Sheet for additional information.

KEY FEATURES OF THE W65C365

* Hi-Rel low power CMOS process
* Operating TA= -55oC to +125oC
* Single 1.2V to 5.5V power supply
* Static to 4 MHz clock operation
* W65C816 compatible CPU
  - --8-, 16-, & 32-bit parallel processing
  - --Variable length stack
  - --True indexing capability
  - --Twenty-four address modes
  - --Decimal or binary arithmetic
  - --Pipeline architecture
  - --Fully static CPU
  - --W65C compatible CPU
* Single chip microcomputer
  - --2 Twin Tone Generators
  - --64 CMOS compatible I/O lines
  - --8K x 8 ROM on-chip
  - --576 x 8 RAM on-chip
  - --WAIt for interrupt
  - --SToP the clock
  - --Fast oscillator start and stop feature
* 16 Mbyte linear address space
* Twenty-nine priority encoded interrupts
  - --BRK software interrupt
  - --RESET "RESTART" interrupt
  - --NMI- Non-Maskable Interrupt
  - --ABORT Interrupt
  - --COP software interrupt
  - --IRQ- level interrupt
  - --8 timer edge interrupts
  - --6 edge interrupts
  - --PIB Interrupt
  - --4 UART Receiver Interrupts
  - --4 UART Transmitter Interrupts
* Four (4) UART's
* Time of Day (ToD) clock features
* 8 x 16 bit timer/counters
* Bus Control Register
  - --Many bus operating features and modes
  - --8 Programmable Chip Select outputs
* Low cost 84 lead plastic packages
* Hi-Rel 84 Lead Ceramic packages
* Macro Assembler available
* C, Basic and Pascal compilers available

SECTION 1

W65C365 FUNCTION DESCRIPTION

1.1 The W65C832S Static 8-, 16-, and 32-bit Microprocessor Core

The W65C832S 32-bit microprocessor is the fully static (may be stopped when PHI2 is high or low) version of the popular W65C816 microprocessor used in the Apple IIgs personal computer system. The W65C832S is compatible with the NMOS 6502 and CMOS 65C02 used in many control applications and personal computers.

The small die size and low power consumption of the W65C832S offer an excellent choice as a cost effective 32-bit core microprocessor in one-chip microcomputers.

The W65C832S instruction set is compatible with the W65C02 and W65C02S, 8-bit microprocessors, W65C802 and W65C816, 16-bit microprocessors.

WDC recommends the following book for more programming information:

Programming the 65816 Including the 6502, 65C02, and 65802
David Eyes and Ron Lichty
Prentice Hall Press
A Division of Simon & Schuster, Inc.
Gulf & Western Bldg.
One Gulf & Western Plaza
New York, NY 10023

1.2 8K x 8 ROM

The W65C365 8K x 8 bit Read Only Memory (ROM) usually contains the user's program instructions, interrupt vectors, and other fixed constants. These are mask-programmed into the ROM during fabrication of the W65C365 device.

1.3 576 x 8 RAM

The 576 x 8 bit Random Access Memory (RAM) contains the user program stack and is used for scratch pad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data.

1.4 Bus Control Register (BCR)

1.4.1 The Bus Control Register (BCR) controls the various modes of I/O and external memory interface.

1.4.2 During power-up the value of BE/RDY defines the initial values of BCR0, BCR3 and BCR7, three bits in the BCR that set up the W65C365 for In-Circuit-Emulation (ICE) or test modes.

1.4.3 When BE/RDY goes high after RES- goes high the BCR sets up the W65C365 for emulation. Port 0 and 1 are the address outputs, Port 2 is the data I/O bus and RUN/SYNC is the multiplexed RUN/SYNC function. (see RUN/SYNC pin function description).

1.4.4 When BE/RDY goes high before RES- goes high, all bits in the BCR are "0".

1.4.5 After RES- goes high BE/RDY no longer effects the BCR register, and BCR may be written under software control to reconfigure the W65C365 as desired.

1.4.6 Table 1-4-1 indicates how BCR7 and BE/RDY define the W65C365 configuration.

Table 1-4-1 BCR7 AND BE/RDY CONTROL

BCR7	BE/ RDY	W65C365 configuration
0	0	Internal ROM External Processor (DMA test mode)
0	1	Internal ROM Internal Processor
1	0	External ROM External Processor (DMA test mode)
1	1	External ROM Internal Processor

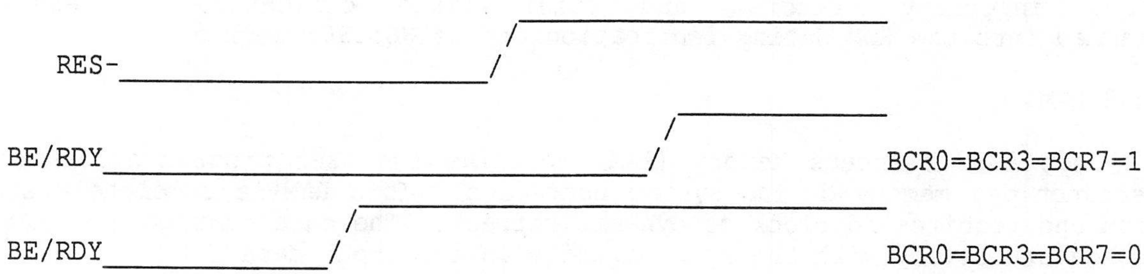


Figure 1-4-1 BE/RDY TIMING RELATIVE TO RES- INPUT

7	6	5	4	3	2	1	0	BCRx

Bit 0 — External Memory Bus Enable
0=Ports 0,1,2,3 are I/O
1=Ports 0,1,2,3 are address and data bus for external memory or I/O access

Bit 1 — Tone Generator 0 (TG0) Enable
0=Disable TG0
1=Enable TG1

Bit 2 — Tone Generator 1 (TG1) Enable
0=Disable TG1
1=Enable TG1

Bit 3 — In-Circuit-Emulation (ICE) Enable
0=RUN/SYNC = RUN, BA/DOD- = BA/1
W65C365 is in normal mode of operation
1=RUN/SYNC = RUN/SYNC , BA-/DOD- = BA-/DOD-,
All on-chip addressed memory or I/O for reads or writes are output on the data bus (this is the emulation mode of operation)

Bit 4 — Monitor "Watch Dog" Enable
0=disable
1=enable

Bit 5 — ABORT enable
0=disable ABORT
1=enable ABORT on P40

Bit 6 — NMI- enable
0=disable NMI
1=enable NMI on P40

Bit 7 — External ROM Enable
0=internal ROM
1=external ROM

Figure 1-4-2 BUS CONTROL REGISTER (BCR)

1.5 The Timers

1.5.1 Upon Timer clock input negative edge the timer counter is decremented by 1.

1.5.2 A write to the timer low counter writes the timer low latch.

1.5.3 A read of the timer high or low counter reads the timer high or low counter.

1.5.4 Upon Timer clock input negative edge when the timer low counter reaches zero, the timer hi counter is decremented by 1. Upon Timer clock input positive edge, when the timer hi counter reaches zero, this sequence occurs:

1.5.4.1 The Timer sets its associated interrupt flag. If the interrupt is enabled the MPU is then interrupted and control is transferred to the vector associated with the interrupt. When Timer 0 times out, the W65C365 is restarted: on-chip logic pulls RES- pin low for 2 CLK cycles and releases RES- to go high, "restarting" the W65C365.

1.5.4.2 The Timer hi counter is loaded from the timer hi latch, and timer low counter is loaded from timer low latch.

1.5.5 A write to the Timer high counter writes to the timer hi latch and this sequence occurs:

1.5.5.1 The timer hi latch is loaded from data bus.

1.5.5.2 The timer low counter is loaded from the timer low latch, and the timer hi counter is loaded from the timer hi latch.

1.5.6 Timer 0 is disabled after RES- and is activated by the first TER0 transistion from "0" to "1" (the first load of Timer 0).

1.5.6.1 The Timer 0 counter is reloaded with the value in the Timer 0 latches when the TER0 bit 0 makes a transition from a "0" to "1". TER0 transition from a "1" to a "0" has no effect on the timer.

Table 1-5 THE TIMER FUNCTIONS

Number	Timer Function	TCR0=0	TCR0=1
T7	Pulse Width Measurement	FCLK	---
T6	Tone Generator	FCLK	---
T5	Tone Generator	FCLK	---
T4	UART Baud Rate or Pulse, Input/Output	FCLK	P60
T3	UART Baud Rate	FCLK	---
T2	Prescaled Interrupt	FCLK/16	---
T1	Time of Day	CLK	---
T0	Monitor Watch Dog	CLK	---

7	6	5	4	3	2	1	0	TCRx

Bit 0 — Timer 4 Input Clock Select
0=FCLK
1=P60

Bit 1 — Timer 4 Output Enable
0=disable
1=enable output on P61

Bits 3, 2 — PWM Edge Interrupt Select on P62

3	2	
0	0	disable
0	1	Positive Edge
1	0	Negative Edge
1	1	Both Edges

Bit 4 — UART0 Timer Select
0=Timer 3
1=Timer 4

Bit 5 — UART1 Timer Select
0=Timer 3
1=Timer 4

Bit 6 — UART2 Timer Select
0=Timer 3
1=Timer 4

Bit 7 — UART3 Timer Select
0=Timer 3
1=Timer 4

Figure 1-5-1 TIMER CONTROL REGISTER (TCR)

```
 ________ ________ ________ ________ ________ ________ ________ ________
|        |        |        |        |        |        |        |        |      0=disable
|   7    |   6    |   5    |   4    |   3    |   2    |   1    |   0    |TERx 1=enable
|________|________|________|________|________|________|________|________|
    |        |        |        |        |        |        |        |
    |        |        |        |        |        |        |        |
    |        |        |        |        |        |        |       Timer 0
    |        |        |        |        |        |        |
    |        |        |        |        |        |       Timer 1
    |        |        |        |        |        |
    |        |        |        |        |       Timer 2
    |        |        |        |        |
    |        |        |        |       Timer 3
    |        |        |        |
    |        |        |       Timer 4
    |        |        |
    |        |       Timer 5
    |        |
    |       Timer 6
    |
   Timer 7
```

Figure 1-5-2 TIMER ENABLE REGISTER (TER)

1.6 Interrupt Flag Registers (TIFR,EIFR,UIFR)

1.6.1 A bit of these registers is set to a "1" in response to an interrupt signal from a source. Sources specified as level-triggered assert the corresponding IFR bit if an edge occurs and is held to a "1" as long as the IRQ- input is held low. Sources specified as edge-triggered assert the corresponding IFR bit upon and only upon transition to the specified polarity. Note that changes for edge-triggered bits are asynchronous with PHI2.

1.6.1.1 Read of an IFR register
A read from an IFR register transfers its value to the internal data bus.

1.6.1.2 Write to an IFR register
A write of a "1" to any bits of these registers disasserts those bits but has no further effect when execution of that write instruction is completed; that is, the bit is reset by a pulse but not held reset. A write of a "0" to any bits of these registers has no effect. (Note that you must write a "1" to the corresponding IFR bit after the interrupt has been serviced; otherwise, the interrupt will continue to occur.)

1.6.1.3 Interrupt Priority
If more than one bit of the Interupt Flag Registers are set to a "1" and enabled, the vector corresponding to the highest memory map location and bit number asserted is used. For example, if both the TIFR1 and EIFR3 were asserted and enabled, then the vector corresponding to EIFR3 would be used. For another example, if both the TIFR3 and EIFR0 were asserted and enabled, then the vector corresponding to EIFR0 would be used.

1.7 Interrupt Enable Registers (TIER,EIER,UIER)

TIER, EIER, and UIER are the interrupt enable registers. Reading an IER register reads its contents and puts the value on the internal data bus. Writing an IER writes a value from the data bus into the register. Setting a bit in an IER to "1" permits the interrupt corresponding to the same bit in the IFR to cause a processor interrupt. Also, if the RUN/SYNC pin was low prior to the interrupt, the pin will go high if BCR3 = 0.

Note that the "I" flag in the microprocessor status register must be cleared with an instruction before any of the interrupts controlled by TIER, EIER, and UIER can occur.

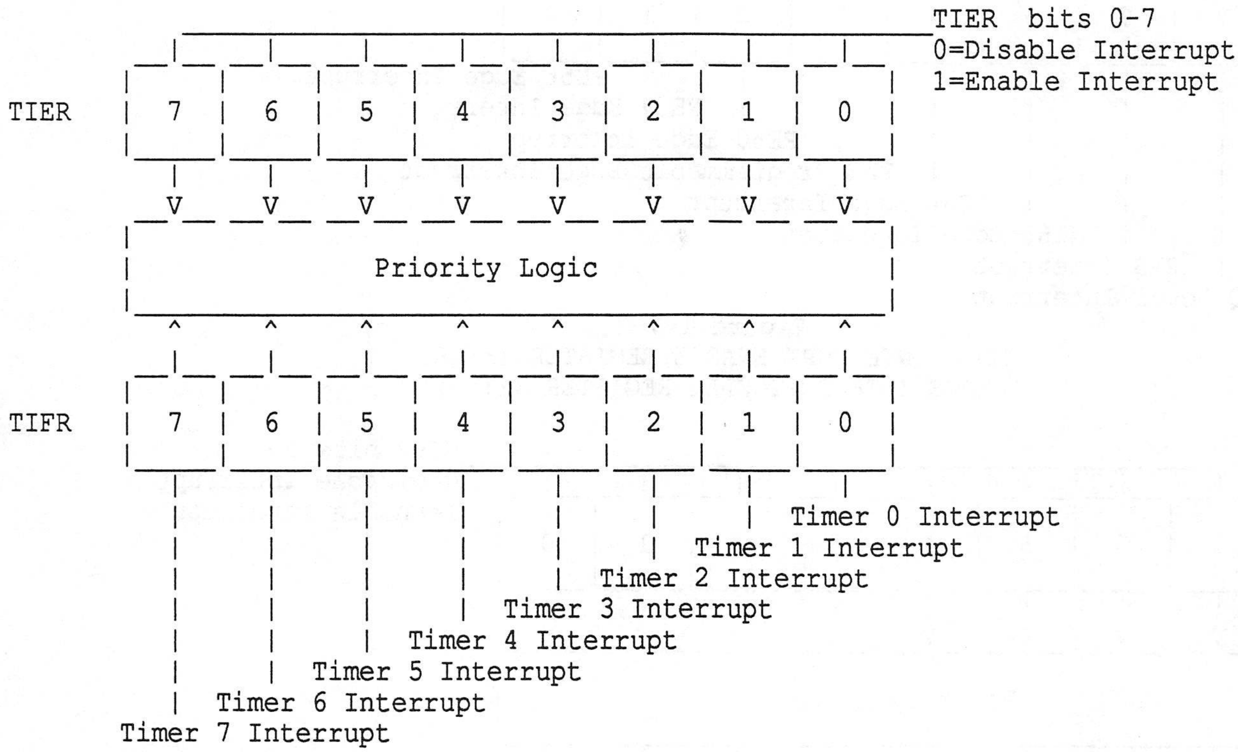


Figure 1-7-1
TIMER INTERRUPT ENABLE REGISTER (TIER)
TIMER INTERRUPT FLAG REGISTER (TIFR)

```
         ______________________________________________________ EIER bits 0-7
       __|__ __|__ __|__ __|__ __|__ __|__ __|__ __|__          0=Disable Interrupt
      |     |     |     |     |     |     |     |     |         1=Enable Interrupt
EIER  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
      |_____|_____|_____|_____|_____|_____|_____|_____|
         |     |     |     |     |     |     |     |
       __V__ __V__ __V__ __V__ __V__ __V__ __V__ __V__
      |                                               |
      |               Priority Logic                  |
      |_______________________________________________|
         ^     ^     ^     ^     ^     ^     ^     ^
       __|__ __|__ __|__ __|__ __|__ __|__ __|__ __|__
      |     |     |     |     |     |     |     |     |
EIFR  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
      |_____|_____|_____|_____|_____|_____|_____|_____|
         |     |     |     |     |     |     |  PE56 Edge Interrupt
         |     |     |     |     |     |  NE57 Edge Interrupt
         |     |     |     |     |  PE60 Edge Interrupt
         |     |     |     |  PWM Programmable Edge Interrupt
         |     |     |  NE64 Edge Interrupt
         |     |  NE66 Edge Interrupt
         |  PIB Interrupt
      IRQ Level Interrupt
```

Figure 1-7-2
EDGE INTERRUPT ENABLE REGISTER (EIER)
EDGE INTERRUPT FLAG REGISTER (EIFR)

```
         ______________________________________________________ UIER bits 0-7
       __|__ __|__ __|__ __|__ __|__ __|__ __|__ __|__          0=Disable Interrupt
      |     |     |     |     |     |     |     |     |         1=Enable Interrupt
UIER  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
      |_____|_____|_____|_____|_____|_____|_____|_____|
         |     |     |     |     |     |     |     |
       __V__ __V__ __V__ __V__ __V__ __V__ __V__ __V__
      |                                               |
      |               Priority Logic                  |
      |_______________________________________________|
         ^     ^     ^     ^     ^     ^     ^     ^
       __|__ __|__ __|__ __|__ __|__ __|__ __|__ __|__
      |     |     |     |     |     |     |     |     |
UIFR  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
      |_____|_____|_____|_____|_____|_____|_____|_____|
         |     |     |     |     |     |     |  UART0R
         |     |     |     |     |     |  UART0T
         |     |     |     |     |  UART1R
         |     |     |     |  UART1T
         |     |     |  UART2R
         |     |  UART2T
         |  UART3R
      UART3T
```

Figure 1-7-3
UART INTERRUPT ENABLE REGISTER (UIER)
UART INTERRUPT FLAG REGISTER (UIFR)

1.8 Asynchronous I/O Data Rate Generation (Timer 3 and 4)

Timer 3 and 4 provide clock timing for the Asynchronous I/O and establishes the data rate for the Serial I/O port. Timer 3 and 4 operate as configured by TCRx and TERx (Timer Control Register and Timer Enable Register) and should be set up prior to enabling the UART.

Table 1-8 identifies the values to be loaded into Timer 3 and 4 to select standard data rates with a clock rate of 4 MHz and 8 MHz. Although Table 1-8 identifies only the more common data rates, any data rate from 1 to 62.5K bps can be selected by using the formula:

$$N = \frac{FCLK}{16 \times bps} - 1$$

where

- N — value to be loaded into timer
- FCLK — the clock frequency
- bps — the desired data rate

Note: One may notice slight differences between the standard rate and the actual data rate. However, transmitter and receiver error of 1.5% or less is acceptable.

Table 1-8 TIMER 3 AND 4 VALUES FOR BAUD RATE SELECTION

Standard Baud Rate	Hexadecimal Value (MHz)		Actual Baud Rate at (MHz)		Clock Rate needed to get Standard Baud Rate (MHz)	
	3.579545	4	3.579545	4	3.579545	4
50	1179	1387	50.00	50.00	3.5792	4.0000
75	0BA6	0D04	75.00	75.01	3.5796	3.9996
110	07F1	08E0	109.99	109.99	3.57984	4.0005
150	05D2	0682	150.05	149.97	3.5784	4.0008
300	02E9	0340	299.89	300.12	3.5808	3.9984
600	0174	01A0	599.79	599.52	3.5808	4.0032
1200	00B9	00CF	1202.80	1201.92	3.5712	3.9936
2400	005C	0067	2405.61	2403.85	3.5712	3.9936
3600	003D	0044	3608.41	3623.19	3.5712	3.9744
4800	002E	0033	4760.03	4807.69	3.6096	3.9936
7200	001E	0022	7216.82	7142.86	3.5712	4.0320
9600	0016	0019	9727.02	9615.38	3.5328	3.9936

1.9 Universal Asynchronous Receiver/Transmitters (UARTs)

The W65C365 Microcomputer provides four full duplex Universal Asynchronous Receiver/Transmitters (UART) with programmable bit rates. The serial I/O functions are controlled by the Asynchronous Communication Control and Status Registers (ACSRx). The ACSRx bit assignment is shown in Figure 1-9-3. The serial bit rate is determined by Timer 3 or 4 for all modes for the UART's. The maximum data rate using the internal clock is 0.5MHz bits per second (FCLK = 8MHz). The Asynchronous Transmitter and Asynchronous Receiver can be independently enabled or disabled.

All transmitter and receiver bit rates will occur at one sixteenth of Timer 3 or 4 as selected.

Whenever Timer 3 or 4 is required as a timing source, it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Table 1-8 for a table of hexadecimal values that represent the desired data rate.

<u>WDC Standard UART Features</u>

* 7 or 8 bit data with or without odd or even parity.
* The Transmitter has 1 stop bit with parity or 2 stop bits without parity.
* The Receiver requires only 1 stop bit for all modes.
* Both the Receiver and Transmitter have priority encoded interrupts for service routines.
* The Receiver has error detection for parity error, framing error, or over-run error conditions that may require re-transmission of the message.
* The Receiver Interrupt occurs due to a receiver data register full condition.
* The Transmitter Interrupt can be selected to occur on either the data register empty (end-of-byte transmission) or both the data register empty and the shift register empty (end-of-message transmission) condition.

1.9.1 Asynchronous Transmitter Operation

The transmitter operation is controlled by the Asynchronous Control and Status Register (ACSRx). The transmitter automatically adds a start bit, parity bit and one or two stop bits as defined by the ACSRx. A word of transmitted data is 7 or 8 bits of data.

The Transmitter Data Register (ARTDx) is loaded on a write. The Receiver is read at the same address.

```
Serial___      ____ ____ ____ ____ ____ ____ ____ ____ ____ ____
Data     |____|____|____|____|____|____|____|____|____|____|    |_
          Start   0    1    2    3    4    5    6    7 Parity Stop
           Bit                                           Bit   Bit
```

The Transmitter Interrupt is controlled by the Asynchronous Control Status Register bit ACSRx1.

IRQAT = ACSRx0((ACSRx1-)(DATA REGISTER EMPTY) + (ACSRx1)(DATA REGISTER AND SHIFT REGISTER EMPTY))

Figure 1-9-1 ASYNCHRONOUS DATA TIMING FOR 8-BIT DATA WITH PARITY

1.9.2 Asynchronous Receiver Operation

The receiver and its selected control and status functions are enabled when ACSRx5 is set to a "1". The data format must have a start bit, 7 or 8 data bits, and one stop bit or one parity bit and one stop bit. The receiver bit period is divided into 16 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit, and a strobe signal is generated at the approximate center of each incoming bit. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. A framing error, parity error or an over-run will set ASCRx7 the receiver error detection bit. An over-run condition occurs when the receiver data register has not been read and new data byte is transferred from the receiver shift register.

```
Serial___      ____ ____ ____ ____ ____ ____ ____ ____
Data     |____|____|____|____|____|____|____|    |    |_
         Start  0    1    2    3    4    5    6  Stop Stop
         Bit                                     Bit  Bit
```

Note: The receiver requires only one stop bit but the transmitter supplies two stop bits for older system timing.

Figure 1-9-2 ASYNCHRONOUS DATA TIMING FOR 7-BIT DATA WITHOUT PARITY

A receiver interrupt (IRQARx) is generated whenever the receiver shift register is transferred to the receiver data register.

1.9.3 Asynchronous Control and Status Registers (ACSRx)

The Asynchronous Control and Status Register (ACSRx) enables the Receiver and Transmitter and holds information on communication status error conditions.

Bit assignments and function of the ACSRx are as follows:

ACSRx0: **Transmitter Enable.** The Asynchronous Transmitter is enabled, the Transmitter Interrupt (IRQATx), and TXDx is enabled on P61 or P63 when ACSRx0=1. When ACSRx0 is cleared, the ACSRx1 is cleared, the transmitter will be disabled, the Transmitter Interrupt will not occur and TXDx will be disabled on P61 or P63. This bit is cleared by a RESET.

ACSRx1: **Transmitter Interrupt Source Select.** When ACSRx1=0, the Transmitter Interrupt occurs due to a Transmitter Data Register Empty condition (end-of-byte transmission). When ACSR=1 the Transmitter Interrupt occurs due to both the Transmitter Data and Shift register empty condition (end-of-message transmission). The Transmitter Interrupt is cleared by writing to the Transmitter Data Register.

ACSRx2: **Seven- or Eight-Bit Data Select.** When ACSRx2=0, the Transmitter and Receiver send and receive 7-bit data. The Transmitter sends a total of 10 bits of information (one start, 7 data, one parity and one stop or 2 stop bits). The Receiver receives 9 or 10 bits of information (one start, 7 data, and one stop or one stop and one parity bits). When writing to the Transmitter in seven bit mode, bit 7 is discarded. When reading from the receive data register during seven bit mode, bit 7 is always zero. When ACSRx2=1, the Transmitter and Receiver send and receive 8-bit data. The Transmitter sends 11 bits of information (one start, 8 data, one parity and one stop or two stop bits). The Receiver receives 10 or 11 bits of information (one start, 8 data, one stop or one parity and one stop bit). Reset clears ACSRx2.

ACSRx3: **Parity Enable.** When ACSRx3=0, parity is disabled. Reset clears ACSRx3. When ACSRx3=1, parity is enabled for both the Transmitter and Receiver.

ACSRx4: **Odd or Even Parity.** When ACSRx4=0 and parity is enabled, then Odd parity is generated where the number of ones is the data register plus parity bit equal an odd number of "1's". When ACSRx4=1 and parity is enabled, then Even parity is generated where the number of ones in the data register plus parity bit equal an even number of "1's". ACSRx4 is cleared by Reset.

ACSRx5: **Receiver Enable.** The Asynchronous Receiver is enabled when ACSRx5=1. Reset clears ACSRx5. When ACSRx5=1 the Receiver is enabled and Receiver Interrupts occur anytime the contents of the Receiver shift register contents are transferred to the Receiver Data Register. The Receiver Interrupt is cleared when the Receive Data Register is read. The Receive Data, RXDx, is enabled on Port 6 when ACSRx5=1. When ACSRx5=0, all Receiver operation is disabled and all Receive logic is cleared, the Receiver data register bits 0-6 are not affected and bit 7 is cleared.

ACSRx6: **Software Semiphore.** ACSRx6 may be used for communications among routines which access the UARTx. This bit has no effect on the UART operation and is cleared upon Reset.

ACSRx7: **Receiver Error Flag.** The Receiver logic detects three possible error conditions and sets ACSRx7: parity, framing or over-run. A parity error occurs when the parity bit received does not match the parity generated on the receive data. A framing error occurs when the stop bit time finds a "0" instead of a "1". An over-run occurs when the last data in the Receiver Data Register has not been read and new data is transferred from the Receive Shift Register. ACSRx7 is cleared by Reset or upon writing a "1" to ACSRx7. Writing a "0" to ACSR7 has not effect on ACSRx7.

```
        _______________________________________________
ACSRx  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
       |_____|_____|_____|_____|_____|_____|_____|_____|
          |     |     |     |     |     |     |     |
          |     |     |     |     |     |     |     Transmitter Enable
          |     |     |     |     |     |     |
          |     |     |     |     |     |     Transmitter Interrupt Source Select
          |     |     |     |     |     |
          |     |     |     |     |     Seven or Eight Bit Data Select
          |     |     |     |     |
          |     |     |     |     Parity Enable
          |     |     |     |
          |     |     |     Odd or Even Parity Select
          |     |     |
          |     |     Receiver Enable
          |     |
          |     Software Semiphore
          |
          Receiver Error Flag
```

Figure 1-9-3 ACSRx BIT ASSIGNMENTS

1.10 The Parallel Interface Bus (PIB)

The Parallel Interface Bus (PIB) is used to communicate instructions and data to and from task oriented processors, smart peripherals, co-processors, and parallel processors.

PIRS 2,1,0 Register Address	Register	
111	7	Automatic Handshake
110	6	
101	5	
100	4	
011	3	Automatic Handshake
010	2	
001	1	PIB Enable Register (PIBER)
000	0	PIB Flag Register (PIBFR)

Register 3 may have a primary role of communicating commands or opcodes between processors.
Register 7 may have a primary role of communicating data or addresses between processors.

Figure 1-10-1 THE PIB REGISTERS

```
        _______________________________________________
       |     |     |     |     |     |     |     |     |
PIBER  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |  0=Disable
       |_(3)_|_(2)_|_(3)_|_(2)_|_(3)_|_(2)_|_(3)_|_(3)_|  1=Enable
          |     |     |     |     |     |     |     |
        __|_____|_____|_____|_____|_____|_____|_____|__
       |     |     |     |     |     |     |     |     |
PIBFR  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
       |_(1)_|_(1)_|_(2)_|_(3)_|_(1)_|_(1)_|_(4)_|_(4)_|
          |     |     |     |     |     |     |     |
          |     |     |     |     |     |     |     |
          |     |     |     |     |     |     |     Enable Parallel Interface
          |     |     |     |     |     |     |     0=Disable PIB
          |     |     |     |     |     |     |     1=Enable PIB
          |     |     |     |     |     |     |
          |     |     |     |     |     |     Enable RD- and WR-
          |     |     |     |     |     |     0=CS- and WE- for WDC bus
          |     |     |     |     |     |     1=RD- and WR- for Intel bus
          |     |     |     |     |     |
          |     |     |     |     |     Automatic Handshake
          |     |     |     |     |     Output Data Available in PIR3 (Reg.3)
          |     |     |     |     |     0=Reset or Host Read of PIR3
          |     |     |     |     |     1=Processor Write to PIR3 and Int.Host
          |     |     |     |     |
          |     |     |     |     Automatic Handshake
          |     |     |     |     Input Data Available in PIR3 (register 3)
          |     |     |     |     0=Reset or Processor Read of PIR3
          |     |     |     |     1=Host Write to PIR3 and Interrupt Processor
          |     |     |     |
          |     |     |     Manual Handshake from Processor
          |     |     |     0=Reset or Write "0" from Processor
          |     |     |     1=Write "1" from Processor and Interrupt Host
          |     |     |
          |     |     Manual Handshake from Host
          |     |     0=Reset or Write "0" from Host
          |     |     1=Write "1" from Host and Interrupt Processor
          |     |
          |     Automatic Handshake
          |     Output Data Available in PIR7 (register 7)
          |     0=Reset or Host Read of PIR7
          |     1=Processor Write to PIR7 and Interrupt Host
          |
          Automatic Handshake
          Input Data Available in PIR7 (register 7)
          0=Reset or Processor Read of PIR7
          1=Host Write to PIR7 and Interrupt Processor
```

Notes:
- (1) Read only from Host or Processor
- (2) Read only from Processor, Read or Write from Host
- (3) Read only from Host, Read or Write from Processor
- (4) Read only from Hose or Processor, will always read back a zero.

Figure 1-10-2 PARALLEL INTERFACE BUS ENABLE (PIBER) AND FLAG (PIBFR) REGISTERS

1.11 Twin Tone Generators

Each Tone Generator(TGx), as shown in figure 1-12-1 is comprised of a sixteen (16) bit timer and a sixteen (16) step divider circuit that selects the proper Digital to Analog (DA) output level. The TGx output sine wave is shown in Figure 1-12-2 below.

$$\text{DA Level } n = E \cos\left(\pi \times (2n+1)/16\right) \quad 0 \le n \le 7$$

$$\text{Register Value } N = \frac{FCLK}{16 \times F} - 1$$

N=value loaded into timer latches
F=desired frequency
FCLK=FCLK input clock

```
             _____________        ______     __________
            |             |      |Divide|   |    DA    |
FCLK-->     |16 bit Timerx|--->  |  by  |---|Converter |---|TGx|
            |_____________|      |__16__|   |__________|
```

Figure 1-11-1 TONE GENERATOR BLOCK DIAGRAM

Table 1-11
COMMUNICATIONS FREQUENCIES GENERATED BY THE
TONE GENERATOR TIMERS 5 AND 6

	Oscillator FCLK = 3.579545 MHz		Oscillator FCLK = 4.000000 MHz	
Standard Frequency (Hz)	Register Value	Actual Frequency (Hz)	Register Value	Actual Frequency (Hz)
	*DTMF Row			
697	320	697	358	696
770	290	769	324	769
852	262	851	292	853
941	237	940	265	940
	*DTMF Column			
1209	184	1209	206	1208
1336	166	1340	186	1337
1477	150	1482	168	1479
1633	136	1633	152	1634
	*Subscriber Tones			
350	638	350	713	350
440	507	440	567	440
480	465	480	520	480
620	360	620	402	620
	*US 110,300 Baud Modem			
1070	208	1070	233	1068
1270	175	1271	196	1269
2025	109	2034	122	2033
2225	100	2215	111	2232
	*European 110,300 Baud Modem			
980	227	981	254	980
1180	189	1177	211	1179
1650	135	1645	151	1645
1850	120	1849	134	1832
	*Teletext			
390	573	390	640	390
450	496	450	555	450
1300	171	1301	191	1302
2100	106	2091	118	2101
	*US 1200 Baud Modem			
390	573	390	640	390
450	496	450	555	450
1200	185	1203	207	1202
2200	101	2193	113	2193

1.12 Processor Defined Cache Control

The Processor Defined Cache Control allows the W65C365 to slow its clock rate. The idea of cache with the W65C365 is that all memory running at the FCLK rate is cache memory. When slower memories are addressed, the PHI2 clock rate is slowed. PHI2 is slowed by extending the PHI2 low and high times. Whether or not the clock rate is slowed down is determined by the System Speed Control (SSCR) Register.

```
 _____ _____ _____ _____ _____ _____ _____ _____
|     |     |     |     |     |     |     |     |
|  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  | SSRx
|_____|_____|_____|_____|_____|_____|_____|_____|
   |     |     |     |     |     |     |     |
   |     |     |     |     |     |     |     |
   |     |     |     |     |     |     |    FCLK Start and Stop Control
   |     |     |     |     |     |     |    0=Stop FCLK
   |     |     |     |     |     |     |    1=Start FCLK
   |     |     |     |     |     |     |
   |     |     |     |     |     |    PHI2 System Timing Clock Select
   |     |     |     |     |     |    0=PHI2 Clock source is CLK (clock)
   |     |     |     |     |     |    1=PHI2 Clock source is FCLK/4 or FCLK
   |     |     |     |     |     |
   |     |     |     |     |    External RAM Select
   |     |     |     |     |    0=Internal RAM (00)0000-01FF
   |     |     |     |     |    1=External RAM (00)0000-01FF
   |     |     |     |     |
   |     |     |     |    System (CS0-CS7) Speed Select
   |     |     |     |    0=Slow (FCLK/4)
   |     |     |     |    1=Fast (FCLK)
   |     |     |     |
   |     |     |    CS4 Speed Select
   |     |     |    0=Slow
   |     |     |    1=Fast
   |     |     |
   |     |    CS5 Speed Select
   |     |    0=Slow
   |     |    1=Fast
   |     |
   |    CS6 Speed Select
   |    0=Slow
   |    1=Fast
   |
  CS7 Speed Select
  0=Slow
  1=Fast
```

Figure 1-12-1 SYSTEM SPEED CONTROL REGISTER (SSCR)

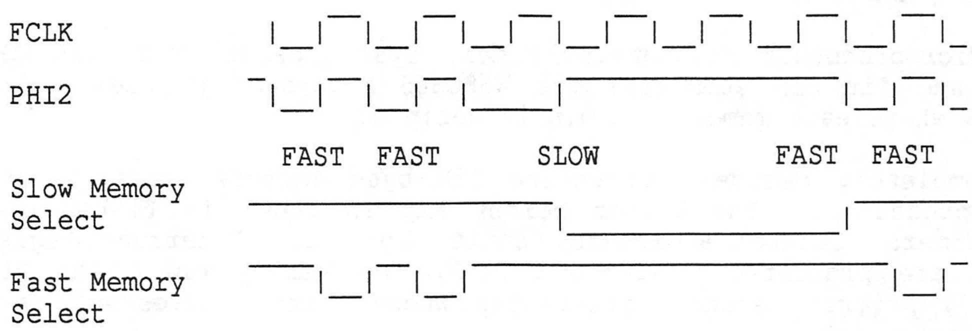


Figure 1-12-2 SYSTEM SPEED CHANGE TIMING DIAGRAM

1.13 Programming Model and Memory Map

The W65C832S Microprocessor Programming Model, System Memory Map, I/O Memory Map, Vector Table, and Pin Map summarize the W65C365 Programming Model and gives the functional area where each memory and pin is defined.

The W65C365 completely decodes the entire 16M byte address space of the on-chip W65C832S microprocessor. The System Memory Map is shown in Table 1-14-1. The on-chip I/O, Timers, Control Registers, Shift Registers, Interrupt Registers, and Data Registers are presented in Table 1-14-2, I/O Memory Map. The W65C365 has twenty-nine (29) priority encoded interrupts whose vector addresses are listed in Table 1-14-3, Vector Table.

8 Bits	8 Bits	8 Bits	8 Bits	

Index and Data Registers

X Register	X
Y Register	Y
ACCUMULATOR	A

Address Registers

0	Program Bank Register (PBR)	Program Counter	PC
0		Direct Register	D
0		Stack Pointer	S
0	Data Bank Register	0	DBR

Status Register

Status	P

Figure 1-13-1 W65C832 Native Mode Programming Model

8 Bits	8 Bits	8 Bits	8 Bits	

Index and Data Registers

		X Register		X
		Y Register		Y
		ACCUMULATOR		A

Address Registers

0	Program Bank Register (PBR)	Program Counter	PC
0		Direct Register	D
0		Stack Pointer	S
0	Data Bank Register	0	DBR

Status Register

			Status	P

Figure 1-13-2 W65C816 16-bit Emulation Programming Model

8 Bits	8 Bits	8 Bits	8 Bits

Index and Data Registers

X Register	X
Y Register	Y
ACCUMULATOR	A

Address Registers

0	Program Bank Register (PBR)	Program Counter		PC
0		Direct Register		D
0		1	Stack Pointer	S
0	Data Bank Register	0		DBR

Status Register

Status	P

Figure 1-13-3 W65C02 8-bit Emulation Programming Model

```
 _________________
| Status Reg.(P) |
| |E|          | |
| |1|          |E|   E16 - W65C816 Emulation
| |6|1|B|      |8|   E8  - W65C02 Emulation
|N|V|M|X|D|I|Z|C|
 | | | | | | | |
 | | | | | | | |__  Carry 1 = true
 | | | | | | |____  Zero 1 = result zero
 | | | | | |______  IRQ- disable 1 = disable
 | | | | |________  Decimal mode 1 = true
 | | | |__________  Index Reg. Select
 | | |____________  Memory Width Select
 | |______________  Overflow 1 = true
 |________________  Negative 1 = neg.
```

Figure 1-13-4 W65C832 Status Register Coding

Table 1-13-1 W65C832 Emulation and Register Width Control

E16	E8	M	X	A and Memory Loads, Stores, Pushes, and Pulls	X,Y Loads, Stores, Pushes, Pulls, and Address Generation	
0	0	0	0	16	32	W65C832 Native
0	0	0	1	16	8	W65C832 Native
0	0	1	0	8	32	W65C832 Native
0	0	1	1	8	8	W65C832 Native
0	1	0	0	32	32	W65C832 Native
0	1	0	1	32	8	W65C832 Native
0	1	1	0	8	32	W65C832 Native
0	1	1	1	8	8	W65C832 Native
1	0	0	0	16	16	W65C816 Emulation
1	0	0	1	16	8	W65C816 Emulation
1	0	1	0	8	16	W65C816 Emulation
1	0	1	1	8	8	W65C816 Emulation
1	1	1	BRK	8	8	W65C02 Emulation

Table 1-14-1 SYSTEM MEMORY MAP

Chip Select	Block Size	Address Range	Function
CS7-	4M	(CO-FF)	User Memory
CS6-	8M	(40-BF)	User Memory
CS5-	4M	(00-3F)	Memory (Note 2)
CS4-	8192	(00)E000-FFFF	ROM Memory (Note 1)
	24320	(00)8000-DEFF	ROM Memory (Note 1)
CS3-	32256	(00)0200-7FFF	Cache Memory (Note 3)
CS2-	64	(FF)FFC0-FFFF	On-chip Interrupt Vectors
	8128	(FF)E000-FFDF	On-chip ROM
	64	(00)DF80-DFBF	On-chip RAM
	16	(00)DF70-FF7F	On-chip Comm. Registers
	32	(00)DF50-FF6F	On-chip Timer Registers
	16	(00)DF40-FF4F	On-chip Control Registers
	8	(00)DF20-DF27	On-chip I/O Registers
	8	(00)DF00-DF07	On-chip I/O Registers
	512	(00)0000-01FF	On-chip RAM
CS1-	64	(00)DFC0-DFFF	COProcessor expansion
CS0-	32	(00)DF00-DF1F	Port replacement & Expansion

Note 1. When on-chip 8K bytes of ROM are enabled, addresses (00)E000-FFFF will not appear in CS4- chip select decode. On Chip addresses (00)DF00-DFFF never appear in CS4- or CS5- chip select decode.

Note 2. When on-chip ROM, CS3- and/or CS4- are enabled, then CS5- decode is reduced by the addresses used by same. CS0- and CS1- address space never appears in CS2-, CS4- or CS5- decoded space.

Note 3. When SSCR2 is "0" (internal RAM), then CS3- is active for addresses (00)0200-7FFF. When SSCR2 is "1" (external RAM), then CS3- is active for addresses (00)0000-7FFF.

Table 1-14-2A I/O REGISTER MEMORY MAP

Address	Label	Function	Reset Value
00DFC0-FF	CS1	COProcessor Expansion	uninitialized
00DF28-3F	---	Reserved	uninitialized
00DF27	PCS7	Port 7 Chip Select	$00
00DF26	PDD6	Port 6 Data Direction Register	$00
00DF25	PDD5	Port 5 Data Direction Register	$00
00DF24	PDD4	Port 4 Data Direction Register	$00
00DF23	PD7	Port 7 Data Register	$FF
00DF22	PD6	Port 6 Data Register	$00
00DF21	PD5	Port 5 Data Register	$00
00DF20	PD4	Port 4 Data Register	$00
00DF08-1F	CS0	Port Replacement & Expansion	uninitialized
00DF07	PDD3	Port 3 Data Direction Register	$00
00DF06	PDD2	Port 2 Data Direction Register	$00
00DF05	PDD1	Port 1 Data Direction Register	$00
00DF04	PDD0	Port 0 Data Direction Register	$00
00DF03	PD3	Port 3 Data Register	$00
00DF02	PD2	Port 2 Data Register	$00
00DF01	PD1	Port 1 Data Register	$00
00DF00	PD0	Port 0 Data Register	$00

Table 1-14-2B CONTROL AND STATUS REGISTER MEMORY MAP

Address	Label	Function	Reset Value
00DF4A-4F	---	Reserved	uninitialized
00DF49	UIER	UART Interrupt Enable Register	$00
00DF48	UIFR	UART Interrupt Flag Register	$00
00DF47	EIER	Edge Interrupt Enable Register	$00
00DF46	TIER	Timer Interrupt Enable Register	$00
00DF45	EIFR	Edge Interrupt Flag Register	$00
00DF44	TIFR	Timer Interrupt Flag Register	$00
00DF43	TER	Timer Enable Register	$00
00DF42	TCR	Timer Control Register	$00
00DF41	SSCR	System Speed Control Register	$00
00DF40	BCR	Bus Control Register	$00/$89

Table 1-14-2C TIMER REGISTER MEMORY MAP

Address	Label	Function	Reset Value
00DF6F	T7CH	Timer 7 Counter High	uninitialized
00DF6E	T7CL	Timer 7 Counter Low	uninitialized
00DF6D	T6CH	Timer 6 Counter High	uninitialized
00DF6C	T6CL	Timer 6 Counter Low	uninitialized
00DF6B	T5CH	Timer 5 Counter High	uninitialized
00DF6A	T5CL	Timer 5 Counter Low	uninitialized
00DF69	T4CH	Timer 4 Counter High	uninitialized
00DF68	T4CL	Timer 4 Counter Low	uninitialized
00DF67	T3CH	Timer 3 Counter High	uninitialized
00DF66	T3CL	Timer 3 Counter Low	uninitialized
00DF65	T2CH	Timer 2 Counter High	uninitialized
00DF64	T2CL	Timer 2 Counter Low	uninitialized
00DF63	T1CH	Timer 1 Counter High	uninitialized
00DF62	T1CL	Timer 1 Counter Low	uninitialized
00DF61	T0CH	Timer 0 Counter High	uninitialized
00DF60	T0CL	Timer 0 Counter Low	uninitialized
00DF5F	T7LH	Timer 7 Latch High	uninitialized
00DF5E	T7LL	Timer 7 Latch Low	uninitialized
00DF5D	T6LH	Timer 6 Latch High	uninitialized
00DF5C	T6LL	Timer 6 Latch Low	uninitialized
00DF5B	T5LH	Timer 5 Latch High	uninitialized
00DF5A	T5LL	Timer 5 Latch Low	uninitialized
00DF59	T4LH	Timer 4 Latch High	uninitialized
00DF58	T4LL	Timer 4 Latch Low	uninitialized
00DF57	T3LH	Timer 3 Latch High	uninitialized
00DF56	T3LL	Timer 3 Latch Low	uninitialized
00DF55	T2LH	Timer 2 Latch High	uninitialized
00DF54	T2LL	Timer 2 Latch Low	uninitialized
00DF53	T1LH	Timer 1 Latch High	uninitialized
00DF52	T1LL	Timer 1 Latch Low	uninitialized
00DF51	T0LH	Timer 0 Latch High	unititialized
00DF50	T0LL	Timer 0 Latch Low	uninitialized

Table 1-14-2D COMMUNICATION REGISTER MEMORY MAP

Address	Label	Function	Reset Value
00DF80-FF	RAM	RAM Registers	uninitialized
00DF7F	PIR7	Parallel Interface Register 7	uninitialized
00DF7E	PIR6	Parallel Interface Register 6	uninitialized
00DF7D	PIR5	Parallel Interface Register 5	uninitialized
00DF7C	PIR4	Parallel Interface Register 4	uninitialized
00DF7B	PIR3	Parallel Interface Register 3	uninitialized
00DF7A	PIR2	Parallel Interface Register 2	uninitialized
00DF79	PIBER	Parallel Interface Enable Reg.	$00
00DF78	PIBFR	Parallel Interface Flag Reg.	$00
00DF77	ARTD3	UART 3 Data Register	uninitialized
00DF76	ACSR3	UART 3 Control/Statis Register	$00
00DF75	ARTD2	UART 2 Data Register	uninitialized
00DF74	ACSR2	UART 2 Control/Statis Register	$00
00DF73	ARTD1	UART 1 Data Register	uninitialized
00DF72	ACSR1	UART 1 Control/Statis Register	$00
00DF71	ARTD0	UART 0 Data Register	uninitialized
00DF70	ACSR0	UART 0 Control/Statis Register	$00

Table 1-14-3 VECTOR TABLE

Address	Label	Function
00FFFE,F	IRQBRK	BRK - Software Interrupt
00FFFC,D	IRQRES	RES - "REStart" Interrupt
00FFFA,B	IRQNMI	Non-Maskable Interrupt
00FFF8,9	IABORT	ABORT Interrupt
00FFF6,7	IRQCOP	COP Software Interrupt
00FFF4,5	IRQRV2	Reserved
00FFF2,3	IRQRV1	Reserved
00FFF0,1	IRQRV0	Reserved
00FFEE,F	IRQAR3	UART3 Receiver Interrupt
00FFEC,D	IRQAT3	UART3 Transmitter Interrupt
00FFEA,B	IRQAR2	UART2 Receiver Interrupt
00FFE8,9	IRQAT2	UART2 Transmitter Interrupt
00FFE6,7	IRQAR1	UART1 Receiver Interrupt
00FFE4,5	IRQAT1	UART1 Transmitter Interrupt
00FFE2,3	IRQAR0	UART0 Receiver Interrupt
00FFE0,1	IRQAT0	UART0 Transmitter Interrupt
00FFDE,F	IRQ	IRQ Level Interrupt
00FFDC,D	IRQPIB	Parallel Interface Bus (PIB) Interrupt
00FFDA,B	IRNE66	Negative Edge Interrupt on P66
00FFD8,9	IRNE64	Negative Edge Interrupt on P64
00FFD6,7	IRPE62	Positive Edge Interrupt on P62 for PWM
00FFD4,5	IRPE60	Positive Edge Interrupt on P60
00FFD2,3	IRNE57	Negative Edge Interrpt on P57
00FFD0,1	IRPE56	Positive Edge Interrupt on P56
00FFCE,F	IRQT7	Timer 7 Interrupt
00FFCC,D	IRQT6	Timer 6 Interrupt
00FFCA,B	IRQT5	Timer 5 Interrupt
00FFC8,9	IRQT4	Timer 4 Interrupt
00FFC6,7	IRQT3	Timer 3 Interrupt
00FFC4,5	IRQT2	Timer 2 Interrupt
00FFC2,3	IRQT1	Timer 1 Interrupt
00FFC0,1	IRQT0	Timer 0 Interrupt

Table 1-14-4A W65C365 84 LEAD PIN MAP

Pin	Name	Control Bit	Signal with Control Bit=0	Signal with Control Bit=1
1	VSS	---	VSS	VSS
2	P56/PE56/ PID6	BCR4 PIBER0	P56	PE56 PID6
3	P57/NE57/ PID7	BCR4 PIBER0	P57	NE57 PID7
4	P60/RXD0/ TIN	ACSR05 TCR1	P60	RXD0 TIN
5	P61/TXD0/ TOUT	ACSR00 TCR0	P61	TXD0 TOUT
6	P62/RXD1/ PWM	ACSR15 TCR2+TCR3	P62	RXD1 PWM
7	P63/TXD1/ TOUT	ACSR10	P63	TXD1
8	P64/RXD2	ACSR25	P64	RXD2
9	P65/TXD2	ACSR20	P65	TXD2
10	P66/RXD3	ACSR35	P66	RXD3
11	P67/TXD3	ACSR30	P67	TXD3
12	RES-	---	RES-	RES-
13	WE-	---	WE-	WE-
14	RUN/SYNC	BCR3	RUN	RUN/SYNC
15	FCLKO-	---	FCLKO-	FCLKO-
16	FCLK	---	FCLK	FCLK
17	BE/RDY	---	BE/RDY	BE/RDY
18	CLK	---	CLK	CLK
19	CLKO-	---	CLKO-	CLKO-
20	PHI2	---	PHI2	PHI2
21	BA/DOD-	BCR3	BA/1	BA/DOD-
22	VSS	---	VSS	VSS
23	VDD	---	VDD	VDD
24	P00/A0	BCR0	P00	A0
25	P01/A1	BCR0	P01	A1
26	P02/A2	BCR0	P02	A2
27	P03/A3	BCR0	P03	A3
28	P04/A4	BCR0	P04	A4
29	P05/A5	BCR0	P05	A5
30	P05/A6	BCR0	P06	A6
31	P07/A7	BCR0	P07	A7
32	P10/A8	BCR0	P10	A8
33	P11/A9	BCR0	P11	A9
34	P12/A10	BCR0	P12	A10
35	P13/A11	BCR0	P13	A11
36	P14/A12	BCR0	P14	A12
37	P15/A13	BCRO	P15	A13
38	P16/A14	BCR0	P16	A14
39	P17/A15	BCR0	P17	A15
40	P30/A16	BCRO	P30	A16
41	P31/A17	BCRO	P31	A17
42	P32/A18	BCRO	P32	A18

Table 1-14-4B W65C365 84 LEAD PIN MAP

Pin	Name	Control Bit	Signal with Control Bit=0	Signal with Control Bit=1
43	VSS	---	VSS	VSS
44	VDD	---	VDD	VDD
45	P33/A19	BCRO	P33	A19
46	P34/A20	BCRO	P34	A20
47	P35/A21	BCRO	P35	A21
48	P36/A22	BCRO	P36	A22
49	P37/A23	BCRO	P37	A23
50	P70/CS0-	PCS70	P70	CS0-
51	P71/CS1-	PCS71	P71	CS1-
52	P72/CS2-	PCS72	P72	CS2-
53	P73/CS3-	PCS73	P73	CS3-
54	P74/CS4-	PCS74	P74	CS4-
55	P75/CS5-	PCS75	P75	CS5-
56	P76/CS6-	PCS76	P76	CS6-
57	P76/CS7-	PCS77	P77	CS7-
58	P20/D0	BCR0	P20	D0
59	P21/D1	BCR0	P21	D1
60	P22/D2	BCR0	P22	D2
61	P23/D3	BCR0	P23	D3
62	P24/D4	BCR0	P24	D4
63	VDD	---	VDD	VDD
64	VSS	---	VSS	VSS
65	P25/D5	BCR0	P25	D5
66	P26/D6	BCR0	P26	D6
67	P27/D7	BCR0	P27	D7
68	TG0	TCR31	---	TG0
69	TG1	TCR33	---	TG1
70	P40/NMI-/ ABORT-	BCR5.BCR6 BCR5.BCR6-	P40	NMI- ABORT-
71	P41/IRQ-	EIER3	P41	IRQ-
72	P42/PII-	PIBER0	P42	PII-
73	P43/PIWE-/ PIWR-	PIBER0.PIBER1- PIBER0.PIBER1	P43	PIWE- PIWR-
74	P44/PICS-/ PIRD-	PIBER0.PIBER1- PIBER0.PIBER1	P44	PICS- PIRD-
75	P45/PIRS0	PIBER0	P45	PIRS0
76	P46/PIRS1	PIBER0	P46	PIRS1
77	P47/PIRS2	PIBER0	P47	PIRS2
78	P50/PID0	PIBER0	P50	PID0
79	P51/PID1	PIBER0	P51	PID1
80	P52/PID2	PIBER0	P52	PID2
81	P53/PID3	PIBER0	P53	PID3
82	P54/PID4	PIBER0	P54	PID4
83	P55/PID5	PIBER0	P55	PID5
84	VDD	---	VDD	VDD

SECTION 2

PIN FUNCTION DESCRIPTION

W65C365 Interface Requirements

This section describes the interface requirements for the W65C365 single chip microcomputer. Figure 2-1 is the Interface Diagram for the W65C365 and Figure 2-2 shows the 84 Lead Chip Carrier pin out configuration.

```
                        _____________________________
                       |                             |
                       | | W65C832S |   | Port 0   | |<8> P0x/Axx
                       | |Static CPU|   |__________| |
                       |                             |
                       | | 576 X 8  |   | Port 1   | |<8> P1x/Axx
                       | |___RAM____|   |__________| |
VDD (4)      -->>      |                             |
RES-         <-->      | | 8192 X 8 |   | Port 2   | |<8> P2x/Dx
WE-          <-->      | |___ROM____|   |__________| |
RUN/SYNC     <<--      |                             |
FCLKO-       <<--      | |Interrupt |   | Port 3   | |<8> P3x/Axx
FCLK         -->>      | |Regs&Logic|   |__________| |
BE/RDY       -->>      |                             |
CLK          -->>      | | Control  |   | Port 4   | |<8> P4x/NMI-/ABORT-,IRQ-,
CLKO-        <<--      | |Regs&Logic|   |__________| |    PIB Control
PHI2         <<--      |                             |
VSS(4)       -->>      | |  Clock   |   | Port 5   | |<8> P5x/PE56,NE57/PIB data
BA/DOD-      <<--      | |__Logic___|   |__________| |
                       |                             |
                       | | 8x16 bit |   | Port 6   | |<8> P6x/UARTx/TIN,TOUT,
                       | |__Timers__|   |__________| |    PWM/PExx, NExx
                       |                             |
                       | | 4x UART's|   | Port 7   | |8>  P7x/CSx-
                       | |__________|   |__________| |
                       |                             |
                       | |   PIB    |   | 2x Tone  | | 2> TGx
                       | |__________|   |Generators| |
                       |_____________________________|
```

Figure 2-1 W65C365 INTERFACE DIAGRAM

```
        P     P        P     P  P
        6     6     P  6  P  5  5
        6     4     6  1  6  7  6
        /     /     2  /  0  /  /
        R     R     /  T  /  P  P                          P  P  P
     P  X  P  X  P  R  X  R  I  I        P  P  P  P  P  P  4  4  4
     6  D  6  D  6  X  D  X  D  D        5  5  5  5  5  5  7  6  5
     7  3  5  2  3  D  0  D  7  6        5  4  3  2  1  0  /  /  /
     /  /  /  /  /  1  /  0  /  /        /  /  /  /  /  /  P  P  P
     T  N  T  N  T  /  T  /  N  P        P  P  P  P  P  P  I  I  I
     X  E  X  E  X  P  O  T  E  E  V  V  I  I  I  I  I  I  R  R  R
     D  6  D  6  D  W  U  I  5  5  S  D  D  D  D  D  D  D  S  S  S
     3  6  2  4  1  M  T  N  7  6  S  D  5  4  3  2  1  0  2  1  0
 ___________________________________________________________________
|                                                                   |
|   11 10  9  8  7  6  5  4  3  2  1 84 83 82 81 80 79 78 77 76 75  |
|                                                                   |
|12 RES-                                          P44/PICS-/PIRD- 74|
|13 WE-                                           P43/PIWE-/PIWR- 73|
|14 RUN/SYNC                                             P42/PII- 72|
|15 FCLKO-                                               P41/IRQ- 71|
|16 FCLK                                          P40/NMI-/ABORT- 70|
|17 BE/RDY                                                   TG1 69|
|18 CLK                                                      TG0 68|
|19 CLKO-                                                 P27/D7 67|
|20 PHI2                       W65C365                    P26/D6 66|
|21 BA/DOD-                    84 LEAD                    P25/D5 65|
|22 VSS                     CHIP CARRIER                     VSS 64|
|23 VDD                                                      VDD 63|
|24 P00/A0                                                P24/D4 62|
|25 P01/A1                                                P23/D3 61|
|26 P02/A2                                                P22/D2 60|
|27 P03/A3                                                P21/D1 59|
|28 P04/A4                                                P20/D0 58|
|29 P05/A5                                              P77/CS7- 57|
|30 P06/A6                                              P76/CS6- 56|
|31 P07/A7                                              P75/CS5- 55|
|32 P10/A8                                              P74/CS4- 54|
|                                                                   |
|   33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53  |
|___________________________________________________________________|

     P  P  P  P  P  P  P  P  P  P  V  V  P  P  P  P  P  P  P  P  P
     1  1  1  1  1  1  1  3  3  3  S  D  3  3  3  3  3  7  7  7  7
     1  2  3  4  5  6  7  0  1  2  S  D  3  4  5  6  7  0  1  2  3
     /  /  /  /  /  /  /  /  /  /        /  /  /  /  /  /  /  /  /
     A  A  A  A  A  A  A  A  A  A        A  A  A  A  A  C  C  C  C
     9  1  1  1  1  1  1  1  1  1        1  2  2  2  2  S  S  S  S
        0  1  2  3  4  5  6  7  8        9  0  1  2  3  0  1  2  3
                                                    -  -  -  -
```

Figure 2-2 W65C365 84 LEAD CHIP CARRIER PIN OUT DESIGNATION

2.1 WE- Write Enable (active low)

The WE- signal is high when the microprocessor is reading data from external memory or I/O and high when it is reading or writing to internal memory or I/O. When WE- is low the microprocessor is writing to external memory or external I/O. The WE- signal is bidirectional; when BE/RDY is low this is an input for DMA operations to on-chip RAM or I/O. When BE/RDY is high the internal microprocessor controls WE-.

2.2 RUN/SYNC RUN and SYNC outputs with WAI and STP defined.

2.2.1 The RUN function of the RUN/SYNC output is pulled low as the result of a WAI or STP instruction. RUN is used to signal an external oscillator to start PHI2. The processor is stopped when RUN is low.

2.2.2 When BCR3=1 (ICE mode), the SYNC function (SYNC=1 indicates an opcode fetch) is multiplexed on RUN/SYNC during PHI2 low time and RUN is multiplexed during PHI2 high time. When BCR3=0 (normal operating mode), the RUN function is output during the entire clock cycle. The ICE module demultiplexes RUN/SYNC to provide full emulation capability for the RUN function.

2.2.3 The BE/RDY input has no effect on RUN/SYNC.

2.2.4 When RUN goes low the PHI2 signal may be stopped when high or low; however, it is recommended PHI2 stop in the high state. When RUN goes high due to an enabled interrupt or reset, the internal PHI2 clock is requested to start. The clock control function is referred to as the RUN function of RUN/SYNC.

2.2.5 The WAI instruction pulls RUN low during PHI2 high time. RUN stays low until an enabled interrupt is requested or until RES- goes from low to high, starting the microprocessor.

2.2.6 The STP instruction pulls RUN low during PHI2 high time and stops the internal PHI2 clock. RUN remains low and the clock remains stopped until RES- goes from low to high.

2.2.7 FCLK can be started or stopped by writing to Timer Control Register One (TCR12) bit 2. When TCR12=0 (reset forces TCR12=0), FCLK is stopped. When TCR12=1, FCLK is started. When starting FCLK oscillator, the system software should wait (100 milliseconds or an appropriate amount of time) for the oscillator to be stable before using FCLK.

2.3 PHI2 Phase 2 Clock Output

PHI2 output is the main system clock used by the microprocessor for instruction timing, general on-chip memory, and I/O timing. PHI2 also is used by the timers when enabled for counting PHI2 clock pulse. The PHI2 clock source is either CLK or FCLK depending on the value of Timer Control Register One bit 1 (TCR11). When TCR11=0, then CLK is the PHI2 clock source. When TCR11=1, then FCLK is the PHI2 clock source.

2.4 CLK, FCLK Clock Inputs (CLKO-, FCLKO- Outputs)

CLK and FCLK inputs are used by the timers for PHI2 system clock generation, counting events or implementing Real Time clock type functions. CLK should always be equal to or less than one-fourth the FCLK clock rate when FCLK is running (see the timer description for more information). CLKO-, FCLKO- outputs are the inverted CLK and FCLK inputs that are used for oscillator circuits that employ crystals or a resistor-capacitor time base. System Speed Control Register bit 1 (SSCR1) selects if CLK (SSCR1=0) or FCLK (SSCR1=1) is used as the PHI2 clock source.

2.5 BE/RDY Bus Enable and RDY Input

2.5.1 BE/RDY controls the address bus, data bus and WE- signals. When RES- goes high signaling in the power-up condition, the processor starts; and if BE/RDY was low when RES- went from low to high then the Bus Control Register (BCR) bits 0, 3, and 7 (BCR0, BCR3, and BCR7) are set to 1 (emulation mode).

2.5.2 After RES- goes high BE/RDY controls the direction of the address bus (A0-A7, A8-A15, A16-A23), data bus (D0-D7) and WE-.

2.5.3 When BE/RDY goes low during PHI2 low time, the address bus and WE- are inputs, providing for DMA (direct memory and I/O access) for emulation purposes. Data from D0-D7 is written to any register addressed by A0-A15 when WE- is low. Data is read from D0-D7 when WE- is high. The W65C832S is stopped when BE/RDY is low.

2.5.4 When BE/RDY is high, the A0-A15, D0-D7 and WE- are controlled by the on-chip microprocessor.

2.5.5 When BE/RDY is pulled low during PHI2 high time, BE/RDY does not affect the direction of the address, data BUS and WE- signals. When BE/RDY is pulled low in PHI2 high time, the W65C832S is stopped so that the processor may be single stepped in emulation.

```
      PHI2‾‾‾\_______________/‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾\______________/‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾\___

            ________   Note 1        Note 1,2       ______________________________
    BE/RDY (DMA)    \____________________________/   normal cycle

    ___________________________      Note 2         ______________________________
    BE/RDY (Emulation)         \______________/      normal cycle
```

Figure 2-5 BE/RDY TIMING RELATIVE TO PHI2

BE/RDY = BE . (RDY + PHI2-) (This logic is on the ICE to provide the emulation interface normally used for W65C832 systems.)

Notes:

1) Address and WE- are inputs with data bus input except when reading on-chip I/O registers or memory. Use this mode for DMA.
2) W65C832S stopped with RDY function of BE/RDY pin. When BCR3=1, the W65C832S read or write of internal I/O register or memory is output on the external data bus so that the internal data bus may be traced in emulation.

2.6 RES- Reset Input/Output (active low)

2.6.1 When RES- is low for 2 or more processor PHI2 cycles all activity on the chip stops and the chip goes into the static low power state.
2.6.2 After a Reset, all I/O pins become inputs. Because of NOR gates on the inputs, RES- disables all input buffers. The inputs may float without having input buffer current flowing while RES- is low. Inputs that are unaffected by RES- are BE/RDY and WE-.
2.6.3 When RES- goes from low to high, RUN/SYNC goes high, the Bus Control Register is initialized to $89 if BE/RDY is low or to $00 if BE/RDY is high. The MPU then begins the power-up reset interrupt sequence in which the program counter is loaded with the reset vector that points to the first instruction to be executed. (See WDC's W65C832S microprocessor data sheet for more information and instruction timing.)
2.6.4 The reset sequence takes 9 cycles to complete before loading the first instruction opcode.
2.6.5 RES- is a bidirectional pin which is pulled low internally for "restarting" due to a "monitor time out", Timer M times out causing a system Reset. (See section 1.5, The Timers for more information.)

2.7 VDD Postive Power Supply

VDD is the positive power supply and has a range of 1.8V to 5.5V for use in a wide range of applications.

2.8 VSS Internal Logic Ground

VSS is the system logic ground. All voltages are referenced to this supply pin.

2.9 Pxx I/O Port Pins

2.9.1 All ports, except Port 7, which is an output Port, are bidirectional I/O ports. Each of these bidirectional Ports has a port data register (PDx) and port data direction register (PDDx). A zero ("0") in PDDxx defines the associated I/O pin as an input with the output transistors in the "off" high impedance state. A one ("1") in PDDxx defines the I/O pin as an output. A read of PDx always "reads" the pin. After reset, all Port pins become input pins with both the data and data direction registers reset to 0.
2.9.2 Port 7 has a Chip Select register (PCS) that is used to enable Chip Selects (CSx-). A "1" in bit x of PCSx enables Chip Select CSx- to be output over P7x while a "0" in PCSx specifies the value in the output data register is to be output on P7x. Port 7 data register is set to all "1's" after Reset, and PCS is cleared to all "0's" after Reset.

2.10 Axx Address Bus

Ports 0, 1, and 3 are also the address bus A0-A23 when configured by the Bus Control Register (BCR). When BCR0 and BCR7 are set to "1" and BCR3=0 (normal operating mode) for external memory addressing, Axx are all "1's" when addressing on-chip memory. When BCR3=1 (ICE mode), the address bus is always active so that the ICE can trace internal read and write operations.

2.11 Dx Data Bus

Port 2 is the data bus D0-D7 when configured by the Bus Control Register (BCR). (See section 1.4 for BCR mode selection.) When BCR0 and BCR7 are set to a "1" and BCR3=0 (normal operating mode) for external memory addressing, Dx are all "1's" when addressing on-chip memory. When BCR3=1 (ICE mode), the data bus is always active so that the ICE can trace internal read and write operations. During external memory cycles the data bus is in the Hi-Z state during PHI2 low time.

2.12 PExx Positive Edge Interrupt inputs

Port pin P56, P60 and P62 have Positive Edge sensitive interrupt inputs (PE56,PE60,PWM) multiplexed with the I/O. The associated bit is set (by an internal one-shot circuit) in the Interrupt Flag Register (IFRx) on a positive transition from "0" to "1". The transition from "1" to "0" has no effect on the IFR. When the associated Interrupt Enable Register bit (IERx) is set to a "1", the MPU will be interrupted provided the interrupt flag bit in the MPU status register P (I flag) is cleared to a "0". When the I flag is "1", interrupts are disabled.

2.13 NExx Negative Edge Interrupt inputs

Port pin P57, P62, P64 and P66 have Negative Edge sensitive interrupt inputs (NE57,PWM,NE64,NE66) multiplexed with the I/O. The associated bit is set (by an internal one-shot circuit) in the Interrupt Flag Register (IFRx) on a negative transition from "1" to "0". The transition from "0" to "1" has no effect on the IFR. When the associated Interrupt Enable Register bit (IERx) is set to a "1", the MPU will be interruped provided the interrupt flag bit in the MPU status register P (I flag) is cleared to a "0". When the I flag is a "1", interrupts are disabled.

2.14 CSx- Chip Select outputs (active low)

The CSx- Chip Select outputs are enabled (individually) as outputs on Port 7 with the PCS register. Each of the eight chip selects is dedicated to one block of external memory defined by the programmable chip select registers; the mapping of each chip select to external addresses is given in Table 1-14-1 System Memory Map.

2.15 IRQ- Level Sensitive Interrupt Request input

The I/O function of port pin P41 is multiplexed with IRQ- Level Sensitive Interrupt input that is selected by Bus Control Register bit 6 (BCR6). When IRQ- is held low the Edge Interrupt Flag Register Bit 7 (EIFR7) is set to a "1". When the Edge Interrupt Enable Register bit 7 (EIER7) is set to a "1" the MPU will be interrupted provided the I flag of the MPU is cleared to a "0" allowing interrupts. Unlike the edge interrupts, which do not hold the interrupt bit set, an interrupt will be generated as long as IRQ- is low.

2.16 NMI-/ABORT- Non-Maskable Edge and ABORT Interrupt Input

The I/O Function of port pin P40 is multiplexed with both the NMI- edge triggered interrupt and the ABORT interrupt. When BCR6=1, the NMI- interrupt is enabled; the MPU will be interrupted on all negative edges of NMI-. Because the I flag cannot prevent NMI- from interrupting, NMI- is thought of as Non-Maskable. When BCR5=1, the ABORT interrupt is enabled. Should both BCR5 and BCR6 be set to "1", both NMI- and ABORT are enabled (normally, this is not desirable).

2.17 RXDx,TXDx Asynchronous Receive Inputs/Transmitter Outputs

The W65C365 has two full duplex Universal Asynchronous Receivers and Transmitters (UARTx) that may be enabled by the Asynchronous Control and Status Registers (ACSRs). When a Receiver is enabled by ACSRx0=1 then port pin P60 or P62 becomes the Asynchronous Receiver Input (RXDx). When a Transmitter is enabled by ACSRx4=1, then port pin P61 or P63 becomes the Asynchronous Transmitter Output (TXDx).

2.18 TIN, TOUT Timer 4 Input and Output

Timer 4 is controlled by TCRx and TERx. When the UART is not in use, Timer 4 can be used for counting input negative pulses on TIN. Timer 4 can also be used to put out a square wave or rectangular wave form on TOUT. When counting negative pulses on TIN the TIN frequency should always be less than one-half the frequency of PHI2. TOUT changes state on every time-out of Timer 4; therefore, varying waveform and frequency depends on the timer latch values and may be modified under software control.

2.19 BA/DOD- Bus Available/Disable Output Data

The BA/DOD- signal is low when the external address (Axx) bus data (Dx) bus is required for operations. While BA/DOD- is high, Axx and Dx may be used for external memory operations such as DMA. BA/1 goes low after the address bus is valid for page mode RAS timing. If an internal cycle is processed than the external bus is available for DMA, etc. and BA stays high. This signal could be thought of as a valid memory address negative edge for sampling the address bus on the negative edge.

2.20 TGx Tone Generator Outputs

The Twin Tone Generator outputs (TGx) are synthesized 16 step cosine waveform outputs as described in Section 1.11 Twin Tone Generators.

2.21 PIB Parallel Interface Bus

2.21.1 The Parallel Interface Bus (PIB) pins are used to communicate between processors in a "star" network configuration or as a co-processor on a "host" processor bus such as an IBM PC or compatible or an Apple II or Mac II personal computer. This PIB may also be used as part of the file server system for large memory systems.

2.21.2 The Parallel Interface Write Enable/Parallel Interface Write (PIWE-/PIWR-) input pin is used with the Parallel Interface Chip Select/Parallel Interface Read (PICS-/PIRD-) signal to transfer data to and from the Parallel Interface Register selected by the Parallel Interface Register select (PIRSx) input pins. When PIWE- and PICS- are configured by the Parallel Interface Bus Enable Register bit 1 (PIBER1=0), then the PIB interface is compatible with WDC microprocessor WE- logical operation with the chip select PICS- input. When PIWR- and PIRD- are selected by PIBER1=1, then the PIB interface is compatible with Intel's microprocessor bus when the chip select is combined with WR- and RD- in the Intel bus configuration.

2.21.3 The PIB interrupt output to the "host" is generated on the Parallel Interface Interrupt (PII) pin. The "host" interrupt is suggested to be received on the IRQ level interrupt input pin of the "host" processor.

2.22 PWM Pulse Width Measurement Input

The Pulse Width Measurement (PWM) input will cause the Timer 7 (T7) counter contents to be transferred to the T7 output latches on the edge(s) selected by the Timer Control Register bits TCR2 and TCR3. The contents of the counter is transferred and an edge interrupt is generated resulting in the EIRF3 being set.

SECTION 3

TIMING, AC AND DC CHARACTERISTICS

3.1 Absolute Maximum Ratings: (Note 1)

Table 3-1 ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to +7.0	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
Operating Temperature	TA	-55 to +125	oC
Storage Temperature	TS	-55 to +150	oC

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may result in permanent damage.
   Functional operation under these conditions is not implied.

3.2 DC Characteristics

VDD = 1.2V to 5.5V (except where noted), VSS = 0V,
TA = -55oC to +125oC (except where noted)

Table 3-2 DC CHARACTERISTICS

	Symbol	Min	Max	Unit
Input High Threshold Voltage				
CLK, FCLK, RES-,	Vih	.9XVDD	VDD+0.3	V
all other inputs		0.7XVDD	VDD+0.3	V
Input Low Threshold Voltage				
CLK, FCLK, RES-,	Vil	VSS-0.3	.1XVDD	V
all other inputs		VSS-0.3	.3XVDD	V
Input Leakage Current (VIN=VSS to VDD, VDD=5.5V) all inputs	Iin	-1	+1	uA
Output High Voltage Ioh=-100uA, VDD=2.8V all outputs	Voh	0.9XVDD	-	V
Output Low Voltage Iol=100uA, VDD=2.8V all outputs	Vol	-	.1XVDD	V
Supply Current (No Load 2.8V	Icc	-	3	mA/MHz
and all on-chip 5.5V circuits operating)		-	6	mA/MHz
Supply Current (No Load) TA= 25oC				
Reset Condition RES-, BE/RDY=VSS; CLK=32768Hz, VDD=5.5V FCLK=HI, PHI2=HI	Ires	-	5	uA
STP Condition CLK=HI, VDD=2.8V FCLK=HI, PHI2=HI	Istp	-	1	uA
Wait for Interrupt Condition CLK=32768Hz FCLK=HI, VDD=2.8V	Iwai	-	5	uA
Capacitance (sample tested) (Vin=0, Ta=25oC, f=1MHz) all pins except VSS, VDD,	Cin	-	10	pF

3.3 AC Characteristics

Table 3-3 AC CHARACTERISTICS

Timing Parameter	Definition
tISA	Address input setup from PHI2
tIHA	Address input hold from PHI2
tODA	Address output delay from PHI2
tOHA	Address output hold from PHI2
tISD	Data input setup from PHI2
tIHD	Data input hold from PHI2
tODD	Data output delay from PHI2
tOHD	Data output hold from PHI2
tISB	BE input setup from PHI2
tIHB	BE input hold from PHI2
tODSY	SYNC output delay from PHI2
tISRR	RDY/RES- input setup from PHI2
tIHRR	RDY/RES- input hold from PHI2
tODRN	RUN output delay from PHI2
tOHRN	RUN output hold from PHI2
tISP	Port input setup from PHI2
tIHP	Port input hold from PHI2
tODP	Port output delay from PHI2
tOHP	Port output hold from PHI2
tISI	Interrupt input setup from PHI2
tIHI	Interrupt input hold from PHI2
tISU	UART Data input setup from PHI2
tIHU	UART Data input hold from PHI2
tODU	UART Data output delay from PHI2
tOHU	UART Data output hold from PHI2
tODD(DMA)	Data output delay from PHI2 (ROM read)
tODPH	PHI2 output delay from CLK/FCLK
tODSC	SCLK output delay from PHI2
tODCSR	CS output delay from PHI2 rising
tODCSF	CS output delay from PHI2 falling
tR	FCLK/CLK risetime
tF	FCLK/CLK falltime
tBR	BE/RDY to RES-
tBV	BE/RDY to D0-7, A0-15, WE-Valid
CEXT	External Capactive load
tCYC	CLK cycle time
tPWL	CLK low time
tPWH	CLK high time
tCYC2	PHI2 cycle time
tPWL2	PHI2 low time
tPWH2	PHI2 high time
tCYCF	FCLK cycle time
tPWLF	FCLK low time
tPWHF	FCLK high time

3.4 AC Parameters

Table 3-4 AC PARAMETERS

Timing Parameter	VDD=1.8V 100 KHz Min	Max	VDD=2.8V 1 MHz Min	Max	VDD=5V+/-10% 2 MHz Min	Max	Units
tISA	3960	-	460	-	210	-	nS
tIHA	20	-	20	-	20	-	nS
tODA	-	2800	-	280	-	180	nS
tOHA	20	-	20	-	20	-	nS
tISD	2700	-	270	-	100	-	nS
tIHD	20	-	20	-	20	-	nS
tODD	-	3300	-	330	-	150	nS
tOHD	10	-	10	-	10	-	nS
tISB	3900	-	390	-	180	-	nS
tIHB	20	-	20	-	20	-	nS
tODSY	-	2700	-	270	-	150	nS
tISRR	700	-	70	-	40	-	nS
tIHRR	20	-	20	-	20	-	nS
tODRN	-	3300	-	330	-	150	nS
tOHRN	20	-	20	-	20	-	nS
tISP	2700	-	270	-	100	-	nS
tIHP	20	-	20	-	20	-	nS
tODP	-	2800	-	280	-	180	nS
tOHP	20	-	20	-	20	-	nS
tISI	800	-	80	-	40	-	nS
tIHI	20	-	20	-	20	-	nS
tISU	#1	-	80	-	40	-	nS
tIHU	#1	-	20	-	20	-	nS
tODU	#1	-	-	300	-	150	nS
tOHU	#1	-	10	-	10	-	nS
tODD(DMA)	-	3800	-	380	-	200	nS
tODPH	-	2000	-	200	-	100	nS
tODSC	#1	-	-	200	-	100	nS
tODCSR	0	1000	0	100	0	50	nS
tODCSF	0	1000	0	100	0	50	nS
tR	-	100	-	100	-	100	nS
tF	-	100	-	100	-	100	nS
tBR	2000	-	200	-	100	-	nS
tBV	-	1900	-	190	-	90	nS
CEXT	50	-	50	-	50	-	pf
tCYC	16000	inf.	4000	inf.	2000	inf.	nS
tPWL	8000	inf.	2000	inf.	1000	inf.	nS
tPWH	8000	inf.	2000	inf.	1000	inf.	nS
tCYC2	TCYCF	inf.	TCYCF	inf.	TCYCF	inf.	nS
tPWL2	.5*TCYC2	inf.	.5*TCYC2	inf.	.5*TCYC2	inf.	nS
tPWH2	.5*TCYC2	inf.	.5*TCYC2	inf.	.5*TCYC2	inf.	nS
tCYCF	4000	inf.	1000	inf.	500	inf.	nS
tPWLF	2000	inf.	500	inf.	250	inf.	nS
tPWHF	2000	inf.	500	inf.	250	inf.	nS

3.5 AC Timing Diagram Notes

1. tCYC must always be equal to or greater than four times tCYCF when FCLK is running.

2. Rise and Fall Times for all signals are measured on a sample basis from .3xVDD to .7xVDD.

   The Rise and Fall times are not programmable on the automated test system that is used for production testing. A typical Rise and Fall time is 5-10ns; therefore, the spec indicates the duty cycle of the clock as tested (tPWL=tCYC/2-tF).

   The Rise and Fall times of 100ns indicate output Rise and Fall times.

   The most critical Rise and Fall times are for PHI2 because all timing is related to PHI2.

   The input Rise and Fall times can affect the input setup time (tIS), output delay time (tOD) and hold time (tH). This must be taken into account in an application. At 2MHz and 4MHz the worst case input Rise and Fall times may prevent a system from working.

3. Hold Time for all inputs and outputs is relative to the associated clock edge.

3.6 AC Timing Diagrams

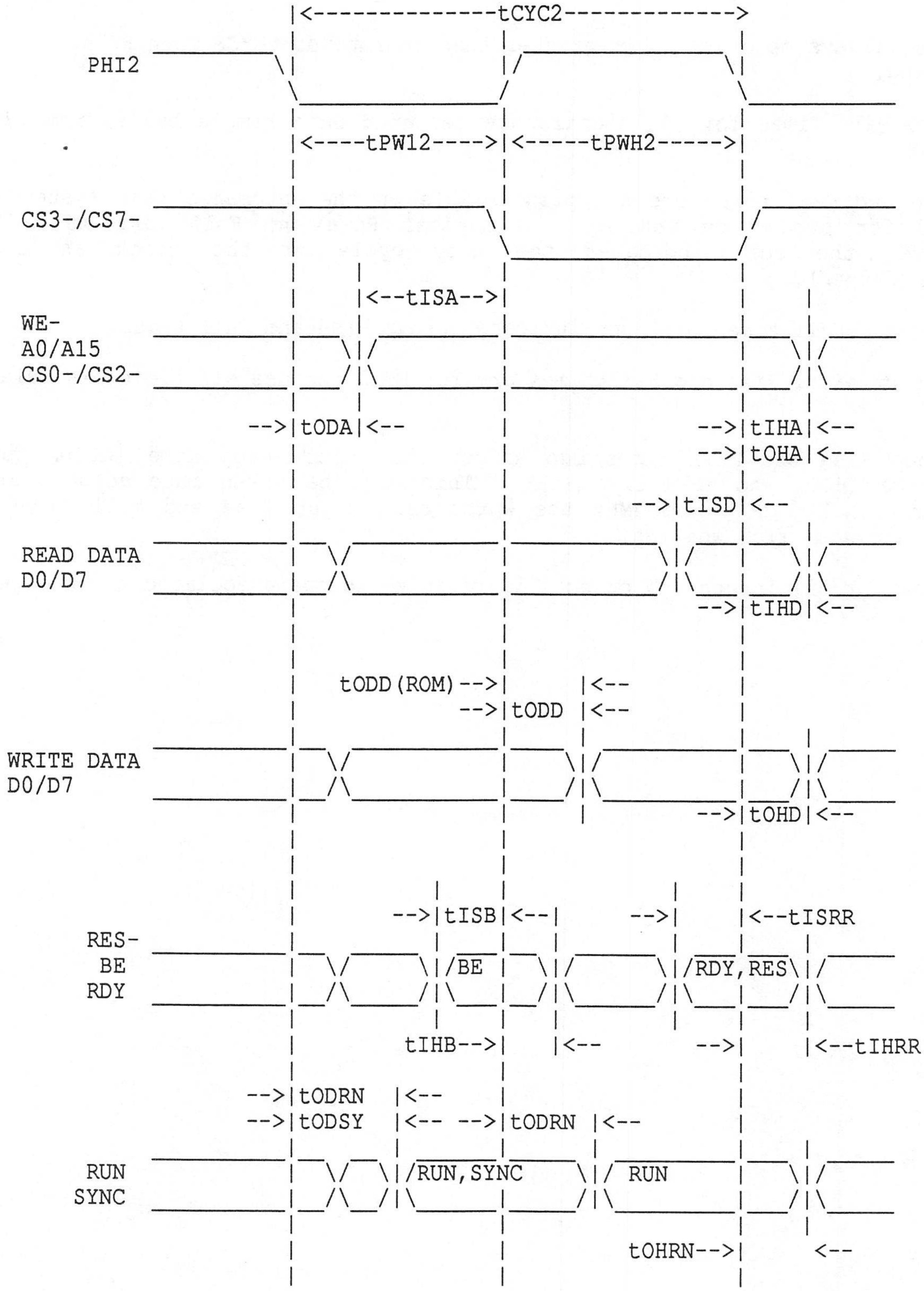
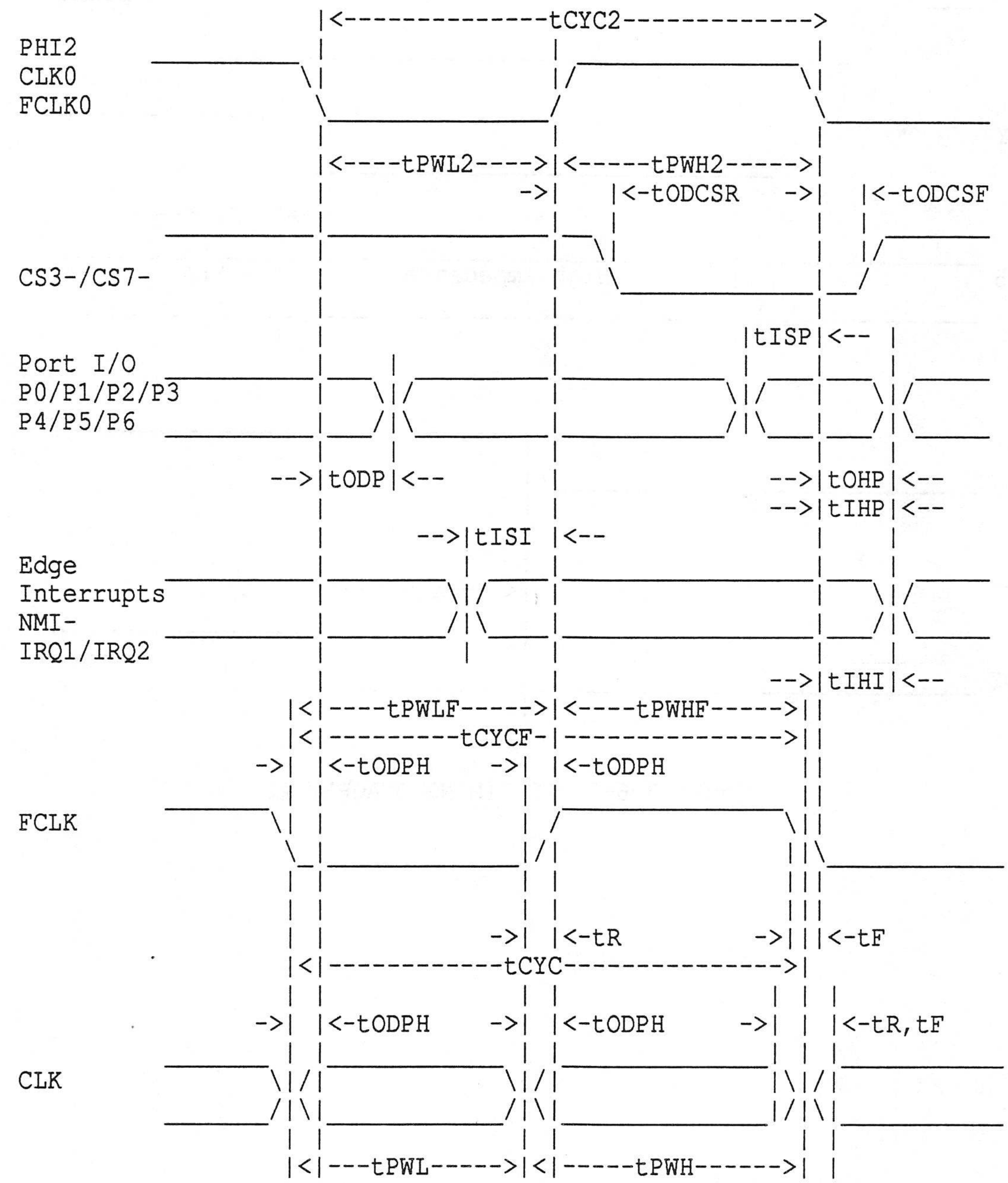


Figure 3-6-1 AC TIMING DIAGRAM #1



Notes:
1. Voltage levels shown are VL = VSS and VH = VDD.
2. Measurement points shown are .5xVDD and .5xVDD.
3. CLK can be asynchronous, tCYC equal or greater than 4xtCYCF.
4. Address and data hold time relative to PHI1 and/or CSx-is 20ns. The PHI2 and CSx- timing is controlled by TCR11. When TCR11=0 PHI12 and CSx- are related to CLK. When TCR11=1, PHI2 and CSx- are related to FCLK.

Figure 3-6-2 AC TIMING DIAGRAM #2

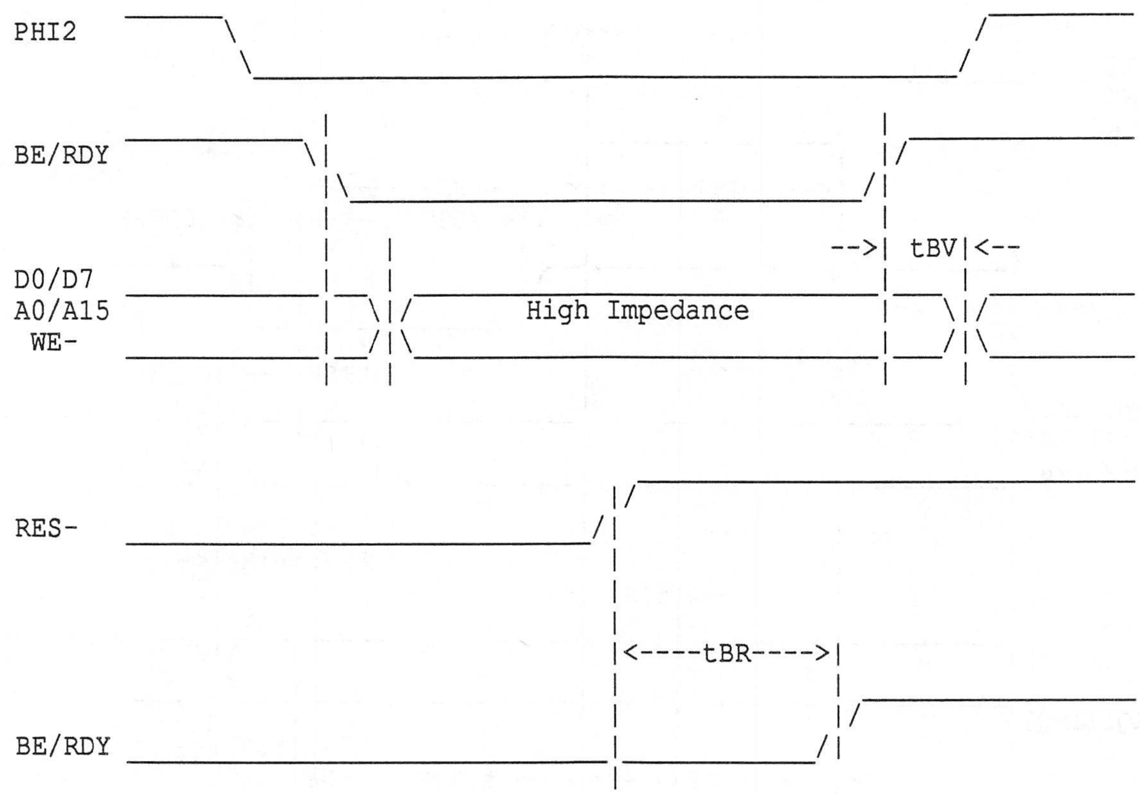


Figure 3-6-3 AC TIMING DIAGRAM #3

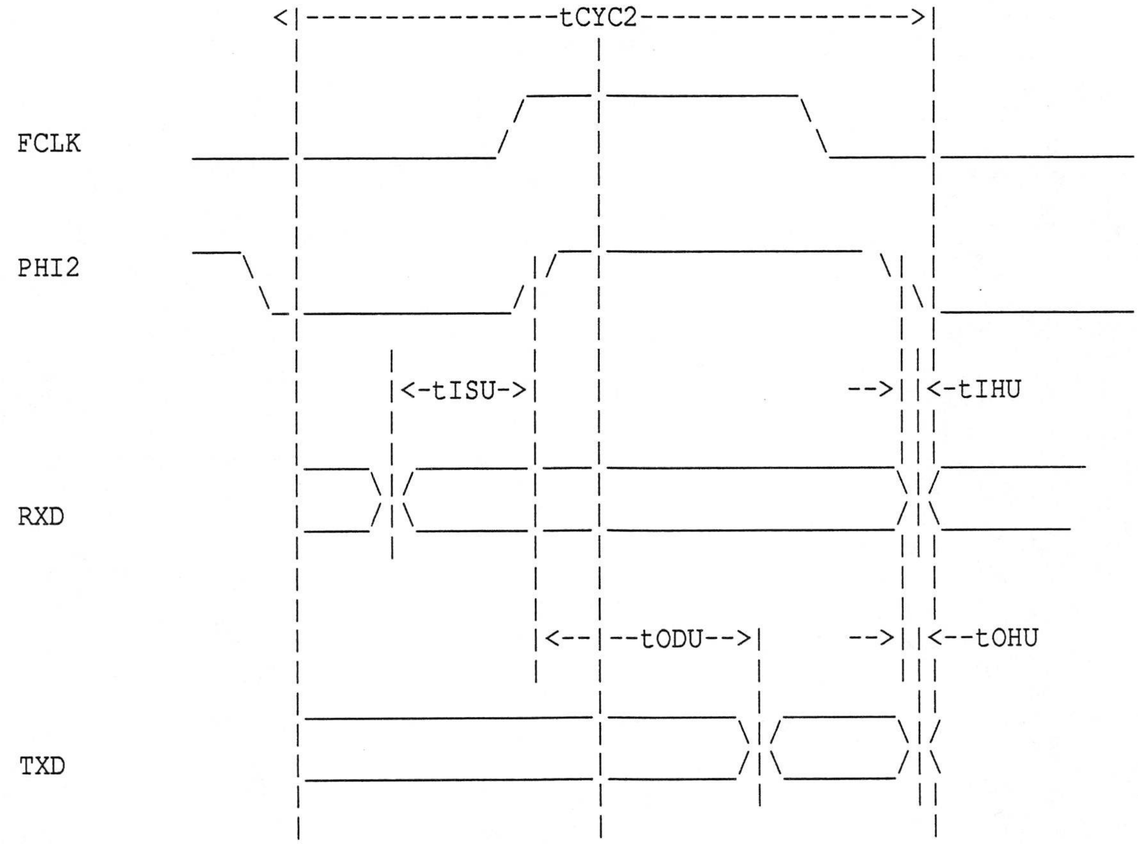


Figure 3-6-4 AC TIMING DIAGRAM #4

SECTION 4

ORDERING INFORMATION

```
                                    W  65C365 C    -2
Description_________________________|    |    |  |  |
W-Standard                               |    |  |  |
                                         |    |  |  |
Product Identification Number____________|    |  |  |
                                              |  |  |
Package_______________________________________|  |  |
P- 84 lead plastic chip carrier                  |  |
C- 84 leadless ceramic chip carrier              |  |
                                                 |  |
Temperature/Processing___________________________|  |
Blank- 0oC to +70oC                                 |
                                                    |
Performance Designator______________________________|
Designators selected for speed and power.
-2 2MHz      -4 4MHz      -6 6MHz      -8 8MHz
```

General sales or technical assistance, and information about devices supplied to a custom specification may be requested from:

The Western Design Center, Inc.
2166 East Brown Road
Mesa, Arizona 85213
Phone: 602-962-4545 Fax: 602-835-6442

WARNING:

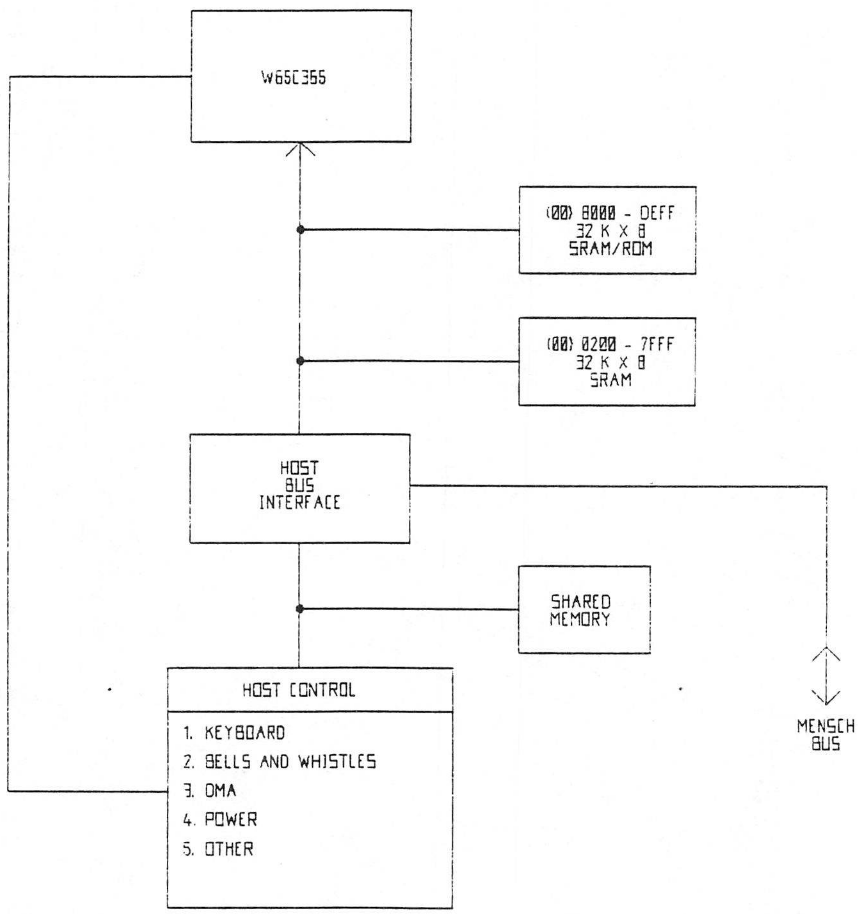
MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

SECTION 5

APPLICATION INFORMATION



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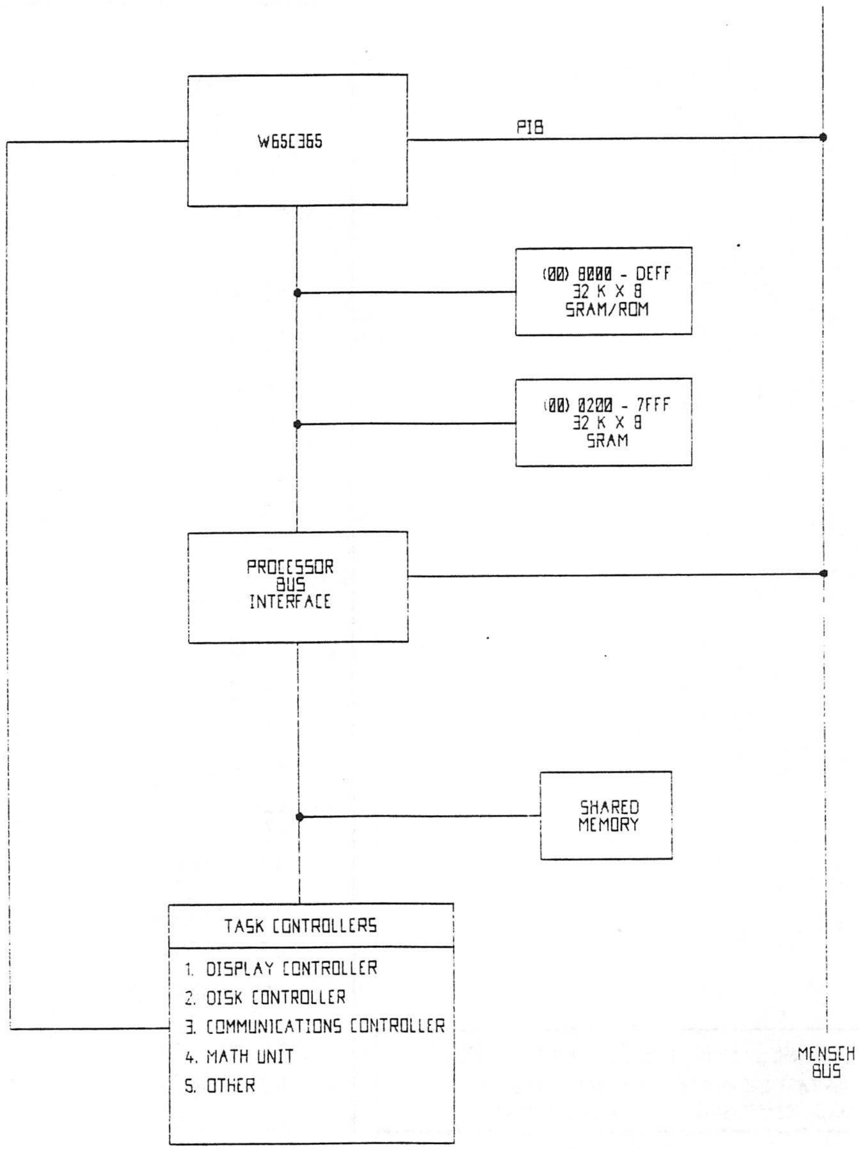
TITLE: MENSCH COMPUTER HOST BLOCK DIAGRAM

DEVELOPMENT MANAGER: DATE:	MANUFACTURING MANAGER: DATE:
WDC ENGINEERING CONTROL DOCUMENT	031591 SHEET 1 OF 4



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TITLE:

MENSCH COMPUTER PROCESSOR BLOCK DIAGRAM

DEVELOPMENT MANAGER: DATE:	MANUFACTURING MANAGER: DATE:
WDC ENGINEERING CONTROL DOCUMENT	031591 SHEET 2 OF 4

1. GND	2. GND
3. + 5V	4. + 5V
5. A0	6. A1
7. A2	8. A3
9. A4	10. A5
11. A6	12. A7
13. A8	14. A9
15. A10	16. A11
17. A12	18. A13
19. A14	20. A15
21. A16	22. A17
23. A18	24. A19
25. A20	26. A21
27. A22	28. A23
29. D0	30. D1
31. D2	32. D3
33. D4	34. D5
35. D6	36. D7
37. RES-	38. WE-
39. BE/RDY	40. PHI2
41. BA/DOD-	42. NMI-/ABORT-
43. RESERVED	44. RESERVED
45. RESERVED	46. RESERVED
47. RESERVED	48. RESERVED
49. RESERVED	50. RESERVED
51. RESERVED	52. RESERVED
53. DMAR0	54. DMAG0
55. DMAR1	56. DMAG1
57. DMAR2	58. DMAG2
59. DMAR3	60. DMAG3
61. IRQ0	62. IRQ1
63. IRQ2	64. IRQ3
65. IRQ4	66. IRQ5
67. IRQ6	68. IRQ7
69. + 5V	70. + 5V
71. GND	72. GND

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TITLE:

MENSCH COMPUTER BUS

DEVELOPMENT MANAGER: DATE:	MANUFACTURING MANAGER: DATE: 031591
WDC ENGINEERING CONTROL DOCUMENT	SHEET 3 OF 4

1. VSS	2. VSS
3. + 5V	4. + 5V
5. A24	6. A25
7. A26	8. A27
9. A28	10. A29
11. A30	12. A31
13. D8	14. D9
15. D10	16. D11
17. D12	18. D13
19. D14	20. D15
21. D16	22. D17
23. D18	24. D19
25. D20	26. D21
27. D22	28. D23
29. D24	30. D25
31. D26	32. D27
33. D28	34. D29
35. D30	36. D31
37. + 5V	38. + 5V
39. VSS	40. VSS

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TITLE: MENSCH COMPUTER BUS EXTENSION FOR 32-BIT DATA AND ADDRESS BUSES

DEVELOPMENT MANAGER:	MANUFACTURING MANAGER:
DATE:	DATE: 031191
WDC ENGINEERING CONTROL DOCUMENT	SHEET 4 OF 4